B.TECH/ECE/6TH SEM/ECEN 3201 (BACKLOG)/2022

DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

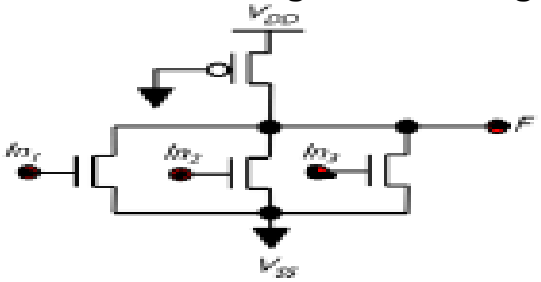
(i) The overall delay is _____ to the relative resistance r.
(a) inversely proportional (b) directly proportional
(c) exponentially proportional (d) independent

(ii) In a CMOS inverter, the direct current path exists from supply voltage (VDD) to ground when both _____ and _____ are turned ON.
(a) NPN and NMOS (b) PMOS and NMOS
(c) PNP and NPN (d) none of these

(iii) Which one of the following processes is preferred to form the gate dielectric (*SiO2*) of MOS transistor?
(a) Sputtering (b) Molecular beam epitaxy
(c) Wet oxidation (d) Dry oxidation.

(iv) VLSI technology uses _____ to form integrated circuit.
(a) transistors (b) switches
(c) diodes (d) buffers

(v) What is the name of the given CMOS logic circuit?



(a) Pseudo-NMOS NOR gate (b) Pseudo-NMOS NAND gate
(c) PMOS only NOR gate (d) NMOS only NOR gate.

(vi) In what region of operation, the MOSFET work as a resistor and current source, respectively?
(a) Linear and saturation (b) Cut-Off and Linear
(c) Saturation and Cut-Off (d) None of these.

(vii) The design flow of VLSI system is
1. architecture design 2. market requirement 3. logic design 4. HDL coding
Choose the correct order
(a) 2-1-3-4 (b) 4-1-3-2 (c) 3-2-1-4 (d) 1-2-3-4.

(viii) What is the logical effort of "R" number of inputs in a NOR logic gate?
(a) 2R/3 (b) (R+1)/3 (c) (2R+1)/3 (d) None of these.

(ix) IDDQ fault occurs when there is
(a) Increased voltage (b) Increased power supply
(c) Increased discharge (d) Increased quiescent current.

(x) CMOS domino logic is same as _____ with inverter at the output line
(a) clocked CMOS logic (b) dynamic CMOS logic
(c) gate logic (d) switch logic

Group- B

2. (a) Design a CMOS gate for the logic function $f(x_1, x_2, x_3)= \Sigma m(1,2,5,7)$. Mention the widths of the NMOS and PMOS for the above design so that the current driving capability remains same as that of the basic CMOS inverter. [(CO1,CO3)(Evaluate/HOCQ)]

(b) Implement Full subtractor circuit using LUT. [(CO2)(Analyze/IOCQ)]

(6 + 2) + 4 = 12

3. (a) Clearly explain the different regions of operation of both pMOS and nMOS transistors in CMOS inverter using VTC curve. Clarify what change in the VTC will be observed if widths of the transistors in the pull up network (PUN) of the inverter is increased. [(CO2)(Remember/LOCQ)]

(b) What do you mean by static and dynamic power dissipation in CMOS inverter circuit?Explain mathematically. [(CO3)(Understand/LOCQ)]

(6 + 3) + 3 = 12

Group - C

4. (a) Draw the circuit diagram of negative edge triggered D flip flop using transmission gate. [(CO4)(Analyze/IOCQ)]

(b) Explain with proper diagram the operation of 1-T DRAM cell. [(CO3)(Remember/LOCQ)]

(c) Draw the CMOS equivalent circuit of S-R latch. [(CO3)(Analyze/IOCQ)]

4 + 5 + 3 = 12

5. (a) Draw the stick diagram for the following expression after applying Euler path algorithm F=$\overline{AB + CD + EF}$. [(CO4)(Create/HOCQ)]

(b) Differentiate between Lambda rule and Micron rule. [(CO2)(Compare/IOCQ)]

9 + 3 = 12

Group - D

6. (a) Draw the block diagram and write a Structural module code for a 8:1 Multiplexer. [(CO2)(Analyze/IOCQ)]

(b) Sketch a schematic circuit described by the following code. Simplify to a minimum number of gates.

```
module exercise   (input  logic a, b, c,
                   output  logic y, z);
assign y= ~a & b & c| a & b & ~c| a & ~b & c;
assign z=a & ~b | ~a & ~b;
endmodule.
```

[(CO1)(Create/HOCQ)]

6 + 6 = 12

7. (a) Discuss the limitations of RTL synthesis. [(CO5)(Remember/LOCQ)]

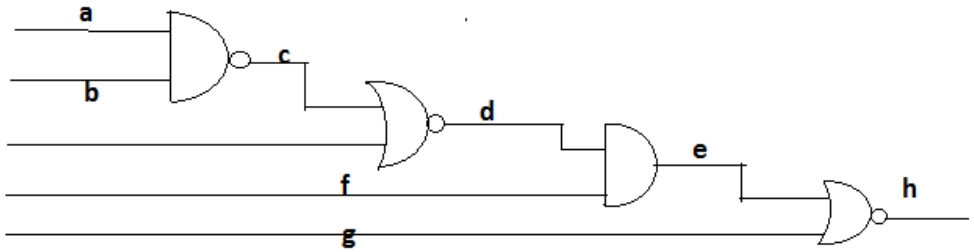
(b) Write an HDL module for a 3:8 Decoder. [(CO5)(Create/HOCQ)]

(c) State with example the types of circuit modelling using HDL. What do you mean by Bit Swizzling? [(CO5)(Analyze/IOCQ)]

2 + 4 + (4 + 2) = 12

Group - E

8. (a) Find the test vectors for the following circuit if it has
(i) stuck-at-1 fault at "f"
(ii) stuck-at-0 fault at "c".



[(CO6)(Analyse/IOCQ)]

(b) Draw a 2 input NAND-gate using CMOS logic and find the test vector if any one pmos is stuck open, and any one nmos is stuck short. Give reasons for your answer. [(CO6)(Analyse/IOCQ)]

6 + 6 = 12

9. Write short notes on any two from the topics given below.
(i) Layout of CMOS inverter [(CO6)(Analyze/LOCQ)]
(ii) VLSI Design flow using Y-chart [(CO2)(Remember/LOCQ)]

(iii) SRAM cell [(CO3)(Remember/LOCQ)]
(iv) Bridging fault [(CO3)(Remember/LOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33	38	29

Course Outcome (CO):

After the completion of the course

1. Students will be able to relate to different MOS structures and functions in order to apply the knowledge in building CMOS circuits
2. Students will learn VLSI Design Cycle, Style and Methodology.
3. Students will be able to determine logic and performance of CMOS combinational and Sequential Circuit including Memory Array Design.
4. Students will be able to construct Physical Layout Design and Stick Diagram of Digital Gates.
5. Students will be able to make use of various synthesis flow and HDL modeling in ASIC Semi Custom Design.
6. Students will be able to interpret Si Testing and Debug related algorithms and Fault Modeling.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question