COMPUTER ORGANIZATION AND ARCHITECTURE
(CSEN 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) In a micro processor, the address of the next instruction to be executed is stored in
(a) Stack Pointer (b) Address Latch
(c) Program Counter (d) General Purpose Register.

(ii) In case of Fully Associative Cache, Conflict miss is
(a) Very High (b) Very low (c) Infinity (d) Zero.

(iii) Memory mapped I/O scheme used for the allocation of address to memories and I/O devices is used for
(a) small system (b) large systems
(c) large and small systems (d) very large systems.

(iv) Interrupt request is acknowledged by the CPU,
(a) immediately as soon as the request is generated
(b) after completion of the current machine cycle
(c) after completion of the current instruction cycle
(d) after completion of the currently executing program.

(v) The basic principle of the Von Neuman computer is
(a) storing program and data in separate memory
(b) using pipeline concept
(c) using a large number of registers
(d) storing both program and data in the same memory.

(vi) In segmentation technique of Virtual Memory, the segment table contains base address as 500 and offset as 200 for page # 2. What is the physical address corresponding to the logical address (2, 250)?
(a) 750 (b) 450 (c) 1000 (d) Gives rise to ERROR.

(vii) The number of cycles required to complete n tasks with k stage pipeline is
(a) k+n-1 (b) k (c) nk+1 (d) none of these.

(viii) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these.

(ix) The two routing functions, Shuffle (S) and Exchange (E), when applied to the binary number 10100111, will result in
(a) 11010011 and 00100111 respectively
(b) 10011101 and 11010011 respectively
(c) 01001111 and 10100110 respectively
(d) 11010011 and 10011101 respectively.

(x) The total number of crossbar modules required in an a^n X a^n delta network is
(a) a^{n-1} / n (b) na^n (c) $(n-1)a^n$ (d) na^{n-1}.

Group- B

2. (a) Evaluate the arithmetic statement E=(X+Y)-(P+Q) using zero address and two address instruction. [(CO4)(Remember/LOCQ)]

(b) What are the advantages of microprogramming control over hardwired control? [(CO2)(Understand/LOCQ)]

(c)

A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program

[(CO1)(Analyze/HOCQ)]

4 + 3 + 5 = 12

3. (a) If each register is specified by 3 bits and instruction *ADD R1,R2,R3* is 2 byte long, then what is the length of op-code field? [(CO2)(Remember/LOCQ)]

(b) Assuming all the registers initially contain 0, what is the value of R1 after the following instruction sequence is executed?

```
MOV  R1, #6
MOV R2,  #5
ADD R3, R1,R1
SUB R1,R3,R2
MULT R3,R1,R1
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[(CO3)(Understand/LOCQ)]

(c) Suppose it takes 7 ns to read an instruction from memory, 3 ns to decode, 5 ns to read the operands from register file, 2 ns to perform the computation of the

instruction and 4 ns to write the results into the register. What is the maximum clock rate of the processor? [(CO2)(Analyse/IOCQ)]

(d) State key differences between CISC and RISC architecture. [(CO1)(Remember/LOCQ)]

3 + 3 + 3 + 3 = 12

Group - C

4. (a) Consider a computer with a byte addressable main memory. The size of the main memory is 2 Kbytes and block size is 16 bytes. The computer employs 32 lines of 4-way set associative cache. Answer the following questions:
   (i) How many lines are there per set?
   (ii) To which set the address 128 (decimal) maps to?
   (iii) The miss scenario takes 25 nsec and a hit scenario takes 5 nsec, when some algorithm is run. If 80% of the processor's memory requests result in a cache hit, how much time does it take to access memory on average? [(CSEN2202.3)(Analyze,Apply/IOCQ)]

   (b) Consider a computer system with a byte addressable physical memory. The logical memory is addressed using 32 bits. The frame size is equal to 2KB. Each entry in the page table is 2 bytes. What is the size of the page table in Mbytes? [(CSEN2202.3)(Analyze,Apply/IOCQ)]

   (c) Consider a reference pattern that accesses a sequence of blocks 0, 4, 0, 2, 1, 8, 0, 1, 2, 3, 0, 4. If the cache uses associative mapping, and LRU algorithm is used for page replacement, find the hit ratio for a cache with four lines. [(CSEN2202.3)(Analyze,Apply/IOCQ)]

   (d) Draw the block diagram of segmentation hardware of virtual memory. [(CSEN2202.3)(Understand,Remember/LOCQ)]

(1 + 1 + 2) + 2 + 3 + 3 = 12

5. (a) What is the main drawback of Programmed IO? How is this drawback overcome in Interrupt-initiated IO? What is the main advantage of DMA over Interrupt-initiated IO? [(CSEN2202.4)(Analyze/IOCQ)]

   (b) (i) Briefly explain, with a diagram, memory-mapped IO.
   (ii) Briefly explain, with examples, vectored and non-vectored interrupts. [(CSEN2202.4)(Understand,Remember/LOCQ)]

   (c) Draw a simple block diagram of DMA controller, showing the registers and their functionalities. Show the connection of this controller with the device participating in the DMA. [(CSEN2202.4)(Understand,Remember/LOCQ)]

(1 + 1 + 1) + (3 + 3) + 3 = 12

Group - D

6. (a) You have the following Instruction Stream coming into a chained Vector Processor
   Load VR , A[3:0]
   Add VR , #1
   Mul VR , #2
   Store A[3:0] , VR

A is a vector if length 4. VR is a Vector register.
Show how the above code is executed in a Vector processor with four pipeline stages (Load / Add / Multiply and Store). [(CO1)(Analyze/IOCQ)]

(b) Explain vector stride and strip mining using examples. [(CO2)(Remember/LOCQ)]

(c) With an example show how the vector processors perform better than scalar processors? [(CO2)(Analyze/IOCQ)]

4 + 4 + 4 = 12

7. Consider the Reservation Table given below:

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

(i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector.
(ii) Draw the state diagram for scheduling the pipeline
(iii) List all simple cycles. Especially point out the Greedy Cycles (GC).
(iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL? [(CSEN2202.2)(Create,Evaluate/HOCQ)]

(3 + 3 + 3 + 3) = 12

Group - E

8. (a) Consider a 4 X 2 Array Processor with 2 numbers of processing elements (PEs) in each of 4 rows and 4 numbers of processing elements (PEs) in each of 2 columns. Load eight numbers 21, 47, 89, 10, 2, 17, 36, 95, in the PEs with snakelike row-major indexing. With the help of diagrams, show the various operations performed in the M(4,2) sorting algorithm to sort the above array. [(CSEN2202.6) (Create, Evaluate/HOCQ)]

(b) Show how the following two matrices can be multiplied in SIMD computer.

$$\begin{pmatrix} 1 & 2 & 3 \\ 4 & 5 & 6 \end{pmatrix} X \begin{pmatrix} 7 \\ 8 \\ 9 \end{pmatrix}$$

[(CSEN2202.6)(Apply,Analyze/IOCQ)]

6 + 6 = 12

9. (a) Draw $3^2 \times 4^2$ Delta network. [(CO6)(Remember/LOCQ)]

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously in a 8X8 Omega network. Does blocking exist in this case? [(CO6)(Analyse/HOCQ)]

(c) Draw the diagram of a 3-stage Cube Interconnection Network. On this diagram clearly show the path between the Source node 4 and the Destination node 3. [(CSEN2202.5)(Understand,Remember/LOCQ)]

3 + (2 + 2 + 1) + (3 + 1) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	40.63	30.21	29.16

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the basic organization of computer and different instruction formats and addressing modes.
2. Analyze the concept of pipelining, segment registers and pin diagram of CPU.
3. Understand and analyze various issues related to memory hierarchy.
4. Understand various modes of data transfer between CPU and I/O devices.
5. Examine various inter connection structures of multi-processor.
6. Design architecture with all the required properties to solve state-of-the-art problems.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question