DIGITAL ELECTRONICS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The range of negative numbers for n-bit signed binary number system is
(a) -1 to $-(2^{n-1}-1)$ (b) 0 to -2^n-1
(c) -1 to -2^{n-1} (d) 0 to -2^n+1.

(ii) A 3 bit adder circuit requires minimum _____
(a) two full adder and two half adder
(b) three full adder
(c) two full adder and one half adder
(d) one full adder and two half subtractor.

(iii) Gray equivalent of the binary code 111001 is
(a) 101101 (b) 100110
(c) 101110 (d) 110011.

(iv) A flip-flop can be used as
(a) frequency divider (b) counter
(c) memory (d) all of the above.

(v) Gray code is advantageous as
(a) moderate switching activity (b) maximum switching activity
(c) minimum switching activity (d) none of the above.

(vi) Racing problem in a J-K flip-flop occurs at
(a) J=K=0 (b) J=1, K=0
(c) J=0, K=1 (d) J=K=1.

(vii) A type of digital circuit technology having highest speed
(a) TTL (b) ECL
(c) CMOS (d) NMOS.

(viii) How many flip-flops are required to make a MOD-17 binary counter?
(a) 17 (b) 6
(c) 5 (d) 4.

(ix) The terminal count of a typical modulus-12 binary counter is _____.
(a) 1000_2 (b) 1011_2
(c) 1011_2 (d) 1101_2

(x) The logic circuit having LOWEST POWER DISSIPATION is _____
(a) TTL (b) ECL
(c) CMOS (d) DTL.

Group - B

2. (a) Realize a 8:1 multiplexer by using 4:1 multiplexer. [(CO3)(Apply/IOCQ)]
(b) Design a 3 bit Gray to Binary code converter circuit. [(CO3)(Create/HOCQ)]
5 + 7 = 12

3. (a) Subtract (6-15) using 5-bit signed binary number representation. [(CO3)(Understand/LOCQ)]
(b) Minimize the logic function Y(A,B,C,D,E) = ∑m(0,1,2,3,8,9,16,17,20,21,24,25,28,29,30,31) by using Karnaugh map. [(CO3)(Apply/IOCQ)]
4 + 8 = 12

Group - C

4. (a) Implement the logic function Y(A,B,C,D) = ∑m(2,4,5,7,10,12,13,15) by using 8:1 multiplexer. [(CO3)(Apply/IOCQ)]
(b) Design a J-K flip flop with truth table by using only NAND gates. [(CO4)(Creat/HOCQ)]
8 + 4 = 12

5. (a) What is the racing problem in J-K flip flop? Explain the remedy of this problem with necessary circuit and wave forms. [(CO4)(Understand/LOCQ)]
(b) What is the difference between flip-flop and latch? [(CO4)(Understand/LOCQ)]
(3 + 6) + 3 = 12

Group - D

6. (a) Design a frequency divider circuit whose output frequency, f_0 is divided by 8 of clock frequency. [(CO4)(Creat/HOCQ)]
(b) Design a 4-bit synchronous up-counter and explain with output waveforms. [(CO4)(Creat/HOCQ)]
6 + 6 = 12

7. (a) Design an asynchronous counter to start the count at 3, also stop the count at 8 and start the count again from 3. [(CO4)(Create/HOCQ)]

(b) Design a 4-bit Johnson counter and explain its operation. [(CO4)(Create/HOCQ)]

6 + 6 = 12

Group - E

8. (a) Implement the given functions using programmable logic array (PLA) X(a,b,c,d) = ∑m(0,2), Y(a,b,c,d) = ∑m(4,6,12,14) and Z(a,b,c,d) = ∑m(4,6,8,10). [(CO5)(Apply/IOCQ)]

(b) Write short notes on successive approximation type ADC and R-2R Ladder type DAC. [(CO5)(Remember/LOCQ)]

6 + (3 + 3) = 12

9. (a) Implement the following logic functions by using PROM.

$A = \sum m(0,2,4,6,8),\ B = \sum m(1,3,5,7)$

[(CO5)(Apply/IOCQ)]

(b) Design a NOR gate using CMOS logic. [(CO6)(Remember/LOCQ)]

7 + 5 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	28	35	37

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the fundamentals of converting from one number system to another.
2. Explain the basic logic operations of NOT, AND, OR, NAND, NOR, and XOR.
3. Analyze, design and implement combinational logic circuits.
4. Analyze, design and implement sequential logic circuits.
5. Describe the nomenclature and technology in the area of memory devices: ROM, PROM, PLD etc. and different kind of ADCs and DACs.
6. Understand the basic operating principles of different logic families.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question