B.TECH/ECE/5TH SEM/ECEN 3104/2020 MICROPROCESSORS AND MICROCONTROLLERS (ECEN 3104)

Time Allotted : 3 hrs

Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and <u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10** × **1** = **10**

(i)	How many address lines are required for an 8K-byte (1024*8=8192 registers) memory chip?			
	(a) 11	(b) 12	(c) 13	(d) 14.
(ii)	The instruction O (a) Program Coun (c) Accumulator	UT cannot send data fr ter	om any register of (b) Register B (d) Flag register.	ther than
(iii)	In POP instruction, after each execution of the instruction, pointer is (a) Incremented by 1 (b) Decremented by (c) Incremented by 2 (d) Decremented by			by 1
(iv)	The number of bi (a) 8	its which is affected by (b) 2	a BSR control wor (c) 1	rd in 8255 is (d) 5.
(v)	When subroutine is called, the address of the instruction next to'CALL' is saved in(a) stack pointer register(b) program counter(c) stack(d) PSW.			
(vi)	LXI B, 2080H is a (a) 1 - byte instru (c) 3 - byte instru	iction	(b) 2 - byte inst (d) 4 - byte inst	

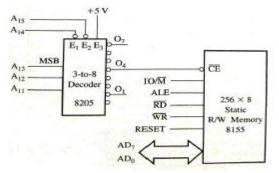
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(vii)	If the crystal with 8085 is 2 MHZ, the time required to execute an			
	instruction of	20 T states is		
	(a) 20µS	(b) 10µS	(c) 40µS	(d) 5µS.
(viii)	The instruction which is used to identify the pending interrupts in			
	8085 is			
	(a) RIM	(b)SIM	(c) DAD	(d) POP.
(ix)	The instruction	n MOV AX, [BX] is a	n example of	
	(a) Indirect ad	dressing	(b) Indexed a	ddressing
	(c) Direct addr	ressing	(d) Based add	lressing.
(x)	The internal RAM memory of the 8051 is			
	(a) 32 bytes	-	(b) 64 bytes	
	(c) 128 bytes		(d) None of th	nese

Group - B

- 2. (a) Why is the data bus bidirectional? Why are the program counter and the stack pointer 16-bit registers? How does the microprocessor differentiate between a data and an instruction?
 - (b) The memory address of the last location of an 8K byte memory chip is FFFFH. Find the starting address?
 - (c) Mention the functions of the Accumulator and the Program counter. (2+2+2)+4+2=12
- 3. (a) What is an addressing mode? How many addressing modes are available in 8085? Explain with proper examples about immediate addressing mode and implicit addressing mode of 8085?



(b) In the above figure, specify the memory address range if the output line 04 of the decoder 8205 is connected to the \overline{CE} signal. Define foldback memory and also specify the range of the foldback memory.

(1+2+3)+6=12

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Group – C

4. (a) Differentiate between Memory-Mapped I/O and Peripheral I/O.

Calculate the total delay in the following program, assuming that the clock frequency of the system is f = 2MHz.

Label	Opcode	Operand
	MVI	C,FFH
LOOP:	DCR	С
	JNZ	LOOP

(b) Explain the bus system of 8085.

3 + 5 + 4 = 12

- 5. (a) Explain the operations of BIU and EU present in 8086 microprocessor.
 - (b) Compare CALL and RET with PUSH and POP instructions in terms of their properties?
 - (c) Define EI and DI in 8085 interrupt?

5 + 5 + 2 = 12

Group – D

- 6. (a) What do you mean by Mode 0, Mode 1 & Mode 2 for 8255 PPI chip?
 - (b) Explain the function of ISR, IRR and IMR in 8259A.
 - (c) List the names of the operating modes of the 8254 programmable interval timer? Define the two new signals available on the 8085 which is introduced due to DMA?

4 + 4 + 4 = 12

- 7. (a) Describe how 8253 is used to generate square waves?
 - (b) Explain the different types of priority modes commonly used under software control in the 8259A?
 - (c) What is the purpose of the operational command words of 8259?

5 + 5 + 2 = 12

Group – E

- 8. (a) Draw the TMOD register of 8051. Explain the function of the mode selection bits. How PSW is used to switch register banks in 8051?
 - (b) Explain the interrupt system of 8051 microcontroller.

3 + (3 + 3) + 3 = 12

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- 9. (a) Show the status of the CY,AC, and P flags after addition of 9CH and 64H in the following instructions.
 MOV A, #9CH
 ADD A, #64H
 - (b) Explain the steps required in enabling an interrupt in 8051.
 - (c) What is the advantage of register indirect addressing mode? Define polling with respect to 8051 microcontroller.

3 + 5 + (2 + 2) = 12

Department & Section	Submission Link	
ECE A	https://classroom.google.com/w/MTQ3NTk4Mjc1MzM1/tc/Mjc0MTY3MjQyNzQ0	
ECE B	https://classroom.google.com/w/MTc1MzExMzk5MTI3/tc/Mjc1MDY3MTY5Njgy	
ECE C	https://classroom.google.com/u/1/w/MTIyMjA0MDMwOTQ1/tc/Mjc0MzgyNjIxOTc3	