MICRO ELECTRONICS AND ANALOG VLSI DESIGN
(ECEN 3103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) At the threshold inversion point, space charge width reaches its
(a) Minimum (b) Maximum
(c) $x_{dT} = N_a/\varphi_{fp}$ (d) $x_{dT}= 2N_a/\varphi_{fp}$.

(ii) Flat - Band voltage is defined as the applied gate voltage such that there is
(a) No band bending in the semiconductor at the oxide – semiconductor interface
(b) No band bending in the oxide at the oxide – semiconductor interface
(c) Zero net space charge in the semiconductor at the oxide – semiconductor interface
(d) Both (a) & (c).

(iii) The low frequency MOS series capacitance in the strong inversion region is
(a) Depletion layer capacitance added in series with insulator capacitance.
(b) Depletion layer capacitance
(c) Insulator capacitance
(d) Depletion layer capacitance added in parallel with insulator capacitance.

(iv) The rms voltage of the sampled noise in a sampling circuit is
(a) $(KT/C)^{1/2}$ (b) $(KT/C)^{-1/2}$
(c)(KT/C) (d) $(KT^{1/2}/C)$.

(v) The channel resistance (r_0) of the MOSFET is related with the channel length modulation parameter (λ)
(a) $r_0 \alpha \lambda$ (b) $r_0 \alpha \lambda^{-1/2}$ (c) $r_0 \alpha \lambda^{-1}$ (d) $r_0 \alpha \lambda^{1/2}$.

(vi) Linear amplification can be obtained from common – source MOSFET amplifier when biased in
(a) Saturation region (b) Linear region
(c) Subthreshold conduction region (d) Only exactly at $V_{DS} = V_{DS\,(sat)}$.

(vii) One of the primary disadvantages of the switched capacitor circuit is
(a) Overlapping clock (b) Nonoverlapping clock
(c) High frequency clock (d) Low frequency clock.

(viii) For amplifier operation, the push – pull inverting CMOS amplifier should have
(a) PMOS in saturation, NMOS in non-saturation
(b) PMOS in non - saturation, NMOS in saturation
(c) PMOS and NMOS both in saturation
(d) PMOS and NMOS both in non-saturation.

(ix) The speed of growth of Si crystals in CZ process is determined by
(a) Ambient temperature
(b) The number of sites on the face of the crystal
(c) The specifics of heat transfer at the interface
(d) Both (b) & (c).

(x) The temperature of the substrate on which the epitaxial layer is grown in the MBE process is in the range of
(a)400^o – 900^o C (b)1500^o – 2000^o C
(c) 373 – 390 K (d)2000^o – 2500^o C.

Group – B

2. (a) Identify the constructional difference between depletion type and enhancement type MOSFET. Explain with proper energy band diagram the key phenomenon behind the principle of operation of the enhancement type MOSFET as a switch.

(b) Derive the expression of the metal – semiconductor work function difference of the MOS structure with the help of the energy band diagram.

(2+4) + 6 = 12

3. (a) Explain the phenomenon of channel length modulation of the MOSFET and correlate this with the different regions of the drain characteristics of the MOSFET.

(b) Show how the output resistance of a MOSFET current sink is increased and derive the expression of the output resistance.

6 + 6 = 12

Group – C

4.(a) Mention the steps in the formation of EGS from MGS. Briefly describe the growth of silicon crystal using CZ process with neat sketch.

(b) Mention the different types of crystal defects.

(4 + 6) + 2 = 12

5.(a) Distinguish between Dry and Wet oxidation.

(b) Why is RTA required? Briefly explain Electromigration phenomenon. Mention few techniques to reduce the problem of junction spiking.

4 + (2+3+3) = 12

Group – D

6. (a) Identify the necessity of small – signal analysis of MOSFET circuits. Interpret the small – signal operation of the enhancement MOSFET amplifier graphically and find the expression of transconductance (g_m) and voltage gain (A_v).

(b) Consider a process technology for which L_{min}=0.4μm, t_{ox}=8 nm, μ_n=450 cm^2/V-s, and V_t=0.7v. Find Cox and kn'.

For a MOSFET with W/L = 8μm/0.8μm, calculate the values of VGS and $V_{DS(min)}$ needed to operate the transistor in the saturation region with a DC current ID=100μA.

All the symbols have their usual significance.

(2 + 4) + 6 = 12

7. (a) Mention the advantages offered by complementary MOS switch. Mention the non-ideal effect associated with a typical current mirror.

(b) Explain the channel charge injection phenomenon and briefly discuss any one of the techniques adopted for charge injection cancellation.

(3 + 3) + (3 + 3) = 12

Group – E

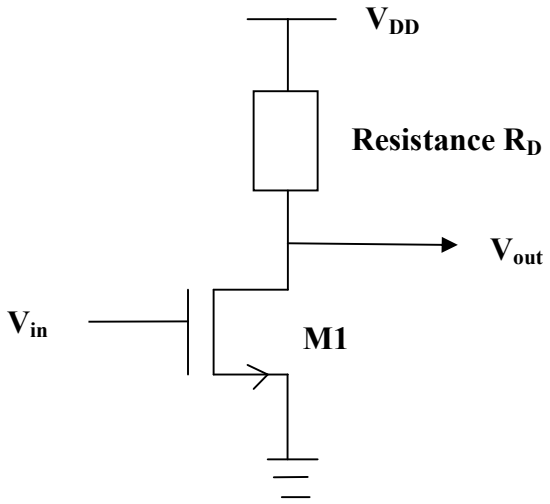
8. (a) Emulate the resistor equivalent of a parallel switched capacitor circuit. For this configuration, if the clock frequency is 100 KHz, find the value of the capacitor C that will emulate a 1MΩ resistor.

(b) Calculate CMRR considering the non-idealities of the practical dual-ended differential amplifier with resistive load.

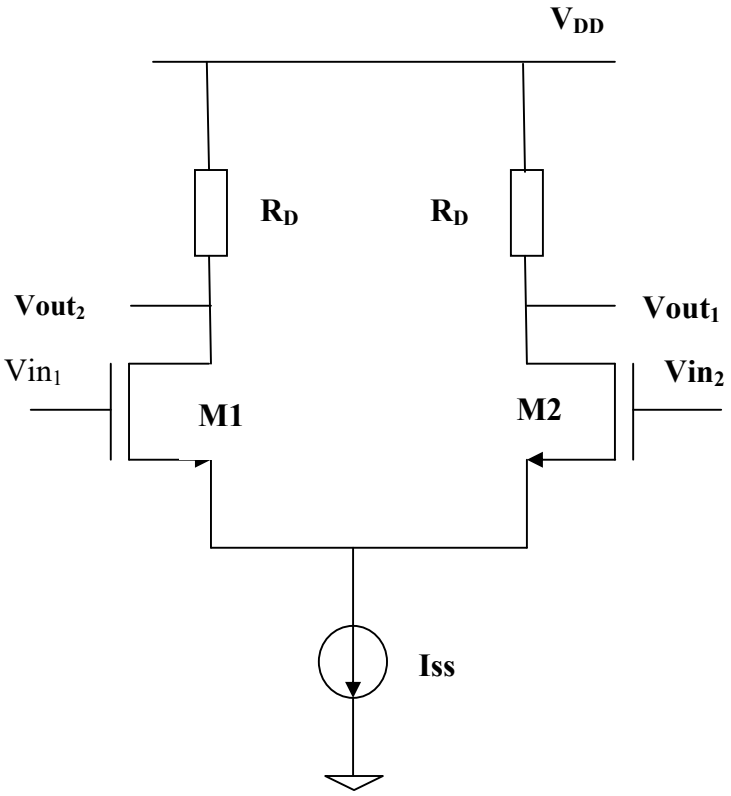
(6+2) + 4 = 12

9. (a) Derive the expression of small – signal output resistance and voltage gain of the common – source active PMOS load inverting CMOS amplifier.

(b) In the given circuit plot the g_m vs. V_{in}



In the following circuit, M2 is twice as wide as M1. Calculate the small – signal gain if the bias values of Vin1 and Vin2 are equal.



6 + 3 + 3 = 12

Department & Section	Submission Link
ECE	https://classroom.google.com/u/0/w/Mjc0NTM3NDU1NDUy/tc/Mjc0NTQxNzk4NjM2