ELECTRONIC DESIGN AUTOMATION
(ECEN 3106)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For sub micron technology the Lgate (channel length) is
(a) > 1 um (b) < 100 nm
(c) > 100 nm (d) None of these.

(ii) Output of physical design is
(a) Schematic (b) Layout
(c) Logical Model (d) RTL.

(iii) Left Edge Algorithm is used for
(a) Floor planning (b) Routing
(c) Placement (d) Partitioning.

(iv) NMOS Transistor in linear region can be modelled as
(a) Resistance (b) Current Source
(c) Open Circuit (d) Voltage Source.

(v) Memory Design is normally done using below Method
(a) Full Custom (b) Std Cell based Semi Custom
(c) FPGA (d) Gate Array.

(vi) With decrease of Vdd, the Delay of an CMOS inverter
(a) Increases (b) Decreases
(c) Remains Same (d) Decreases and then increases.

(vii) The enhancement NMOS type Transistor is basically termed as normally 'OFF" Transistor which becomes "ON" only with
(a) Large positive gate voltage
(b) Large negative gate voltage
(c) Large positive drain voltage
(d) Large negative drain voltage.

(viii) Minimum Number of Transistors in CMOS logic Y = ABC + D is
(a) 12 (b) 6 (c) 14 (d) 10.

(ix) Ideal MOS Channel Resistance value in Saturation is
(a) 0 Ohm (b) Infinite
(c) 10K Ohm (d) 1M Ohm.

(x) A stick diagram represents the design of
(a) Logic (b) Circuit
(c) Layout (d) Architecture

Group – B

2. (a) What are the various capacitance components of a MOS transistor?

(b) Draw the VTC (Voltage Transfer Curve) of a CMOS inverter.

(c) Illustrate how VTC of a CMOS inverter will change if the channel width of the PMOS transistor is increased.

(d) If a CMOS inverter have parameters VOH = 5V, VOL = 0V, VIH = 3.1V, VIL = 2.3V, then what is the value of NMH and NML ?

4+ 3+ 3 + 2= 12

3. (a) Implement a two input OR gate using pass transistor logic.

(b) Implement a two input XOR gate using transmission gate (TG) logic.

6 + 6= 12

Group – C

4. (a) Draw the Y Chart for VLSI Design.

(b) Write a Verilog code for the behavioural model of a D –flip flop.

(c) How a flip flop can be implemented using a latch?

5 + 4 + 3 = 12

5. (a) What is Moore's Law?

(b) What is the number of transistors in a GSI chip ?

(c) Draw the schematic of 3 input NAND gate.

(d) Draw the stick diagram of the same 3 input NAND gate.

2+ 2 +3 + 5= 12

Group – D

6. (a) Draw flow diagram of logic synthesis.

(b) Draw BDD diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a < b< c.

(c) Create the ROBDD diagram and the corresponding optimized Boolean expression.

4+ 4 +4 = 12

7. (a) For the Floor Planning problem, what are the inputs, outputs and the objective (cost) function ?

(b) Formulate the Global Routing problem using the Steiner Tree algorithm.

6 + 6= 12

Group – E

8. (a) Write the Verilog code for behavioural modelling of a 3 input NOR gate.

(b) Draw the flow diagram of high level synthesis.

6 + 6 = 12

9. Write short notes on the following topics
   i) Enhancement mode MOS Transistor
   ii) Technology Library Mapping for Logic Synthesis
   iii) Left Edge Algorithm for Detailed Routing

4+ 4 + 4 = 12

Department & Section	Submission Link
CSE A	https://classroom.google.com/c/MTM4MTA3MzcwMjY3/a/MjcxNTEzNDczNjkz/details
CSE B	https://classroom.google.com/c/MTM4MTA3MzcwMzIy/a/MjcxNTEzMTQzMjY5/details
CSE C	https://classroom.google.com/c/MTMwMDQzNzUzMTY3/a/MjcxNTEzMTQzMTkz/details