COMPUTER ARCHITECTURE
(CSEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The number of cycles required to complete n tasks with k stage pipeline is
(a) K + n -1 (b) k (c) nk + 1 (d) none of these.

(ii) A 64 input Omega Network requires how many stages of 2 x 2 switches?
(a) 6 (b) 64 (c) 8 (d) 4.

(iii) For two instructions I and J WAR hazard occur, if
(a) $R(I) \cap D(J) \neq \varnothing$ (b) $R(I) \cap R(J) \neq \varnothing$
(c) $D(I) \cap R(J) \neq \varnothing$ (d) none of these.

(iv) CC-NUMA stands for
(a) Cache coherent NUMA (b) Cyclical Co-ordination NUMA
(c) Cache Co-ordinated NUMA (d) None of the above.

(v) Which of the following types of instructions are useful in handling sparse matrices in vector processing applications?
(a) Vector- scalar instruction (b) Vector – memory instruction
(c) Masking instruction (d) Scatter – gather instruction.

(vi) Which of the following has no practical usage?
(a) SISD (b) SIMD (c) MISD (d) MIMD.

(vii) Cache memory
(a) increases performance (b) decreases performance
(c) increases machine cycle (d) none of these.

(viii) Utilization pattern of successive stages of a synchronous pipeline can be specified by
(a) truth table (b) excitation table
(c) reservation table (d) periodic table.

(ix) The prefetching is a solution for
(a) Data hazard (b) Structural hazard
(c) Control hazard (d) none of these.

(x) Which of the following is an example of 2-dimensional topologies in static network?
(a) Mesh (b) $3c^3$ network
(c) Linear Array (d) none of these.

Group – B

2.

	1	2	3	4
S1	X			X
S2		X		
S3			X	

Consider the above reservation table. Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline? Find out simple cycle, greedy cycle and MAL? What are the bounds of MAL?

(2 + 4 + 4 + 2) = 12

3. (a) How can hazard occur in executing the following set of instructions?
I1: MOV R1,A ; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP
All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

(b) Differentiate between Von Neuman and Harvard Architecture, explain with schematic diagram.

6 + 6 = 12

Group – C

4 (a) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} Ai \text{ for } k = 0, 1, 2 \ldots N-1.$$

(b) Explain Multistage implementation of a Cube Network with a suitable diagram.

6 + 6 = 12

5. (a) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously in a 8X8 Omega network. Does blocking exist in this case?

(b) Show how the following two matrices can be multiplied using ILLIAC-IV network?

$$\begin{bmatrix} 1 & 2 \\ 4 & 5 \end{bmatrix} \begin{bmatrix} 4 & 7 \\ 7 & 6 \end{bmatrix}$$

(3 + 3 + 1) + 5 = 12

Group – D

6. (a) Draw 3^2 X 4^2 Delta network.

   (b) Write down algorithm for odd- even transposition sort and explain it using a set of data.

6 + 6 = 12

7. (a) Briefly explain the butterfly network.

   (b) Calculate the speedup factor for superscalar architecture and superpipelined architecture.

6 + (3 + 3) = 12

Group – E

8. (a) Draw data flow graph for the following set of instructions:

X = A+B
Y=X/B
Z=A∗X
M=Z−Y
N=Z∗X
P=M/N

   (b) Briefly explain three memory consistency models.

6 + 6 = 12

9. (a) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program.

   (b) What is cache coherence problem? Suggest methods used to solve cache coherence problem.

6 + (2 + 4) = 12

Department & Section	Submission link:
CSE	https://classroom.google.com/w/MjgyNTI3NDEyMjc2/tc/MjgyNTI3NDM2MzYx