VLSI DESIGN AUTOMATION
(ECEN 4181)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The target of IC Design and Fabrication is
(a) Less area and low cost (b) High speed
(c) Less power (d) all of the above.

(ii) For a 180 nm process technology, the value of λ (lambda) is
(a) 90 nm (b) 9nm (c) 180 nm (d) 360 nm.

(iii) The output load capacitance of a CMOS inverter includes
(a) parasitic capacitances
(b) interconnect capacitance
(c) gate capacitance of the subsequent gate
(d) all of the above.

(iv) The tasks of high-level synthesis include
(a) compilation and transformation only
(b) scheduling, allocation and binding only
(c) compilation and scheduling only
(d) both (a) and (b).

(v) RTL is expressed in
(a) VHDL (b) Verilog
(c) Both (a) & (b) (d) None of the above.

(vi) Detailed routing includes
(a) Channel routing (b) Switchbox routing
(c) Both (a) & (b) (d) None of the above.

(vii) In standard cell based design, each cell layout is designed with fixed
(a) Width (b) Height
(c) Both (a) & (b) (d) None of the above.

(viii) Logic synthesis is the process that takes place in the
(a) Transition from the transistor level to the register-transfer level
(b) Transition from the register-transfer level to the transistor level
(c) Floorplanning
(d) Routing.

(ix) KL Algorithm is used for
(a) Partitioning (b) RTL synthesis
(c) Routing (d) Floorplanning.

(x) A pull-down network (PDN) connects an output node to
(a) V_{DD} (b) ground
(c) input (d) all of the above.

Group – B

2. (a) Explain the operation of a NOR gate using NMOS logic.

(b) What is a 'pull up' and a 'pull down' network in CMOS technology? Justify how an NMOS and a PMOS can be used as a pull down and a pull up device.

4 + (2 + 6) = 12

3. (a) Design a Half adder circuit using CMOS logic.

(b) Design a 2:1 MUX using CMOS transmission gates.

8 + 4 = 12

Group – C

4. (a) Explain the Y-chart for VLSI design flow.

(b) Draw the flowchart showing generalized design flow and identify the blocks corresponding to front end and back end design. Briefly explain RTL synthesis.

6 + (4 + 2) = 12

5. (a) Mention the advantages provided by programmable logic devices ? Briefly describe the functionality of PLA.

(b) Implement the following function using AND / OR plane PLA
F1 = ab'd'e+a'b'c'd'e'+bc+de
F2 = a'c'e
F3=bc+de+c'd'e'+bd
F4=a'c'e+ce

(4 + 4) + 4 = 12

Group – D

6. (a) What is High Level Synthesis(HLS)? Draw a flow chart showing the tasks involved in a typical HLS.

(b) What are the main hardware units that are involved in an HLS?

(2 + 5) + 5 = 12

7. (a) What do you understand by partitioning? Briefly discuss the parameters to be addressed to enhance the partitioning efficiency. Mention the classification of partitioning algorithm on the basis of process used for partitioning.

(b) Briefly explain the steps of Kernighan – Lin algorithm. Apply this algorithm for the graph shown in Fig. 1. to identify the vertex pairs to be exchanged and evaluate the gain in the first swap.

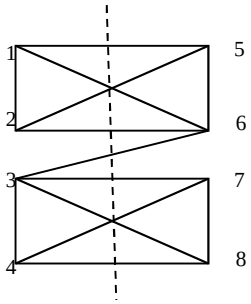

Fig. 1

(1+3+2) + (3+3) = 12

Group – E

8. (a) Illustrate the concept of BDD, OBDD and ROBDD with the representation of the majority function given below :

x1	x2	x3	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(b) Mention the different levels of abstraction in EDA flow.

9 + 3 = 12

9. (a) What is the importance of Technology Mapping ? Briefly discuss the concept of subject DAG, pattern DAG and cover.

(b) Explain the restrictions of any cover and illustrate with suitable example.

(2 + 4) + 6 = 12

Department & Section	Submission Link
AEIE /CSE	https://classroom.google.com/w/MTM4NTU5MjYwMzgz/tc/Mjc0ODE2ODgzMDgx