M.TECH/VLSI/1ST SEM/VLSI 5132/2021

VLSI IC FABRICATION
(VLSI 5132)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Heavily doped polysilicon is deposited using
(a) chemical vapour decomposition (b) chemical vapour deposition
(c) chemical decomposition (d) dry deposition

(ii) Optical masking is used for
(a) pattern transfer (b) protection
(c) cleaning (d) none of the above

(iii) Oxidation in VLSI fabrication industry may be
(a) Dry oxidation (b) Wet oxidation
(c) Both (a) & (b) (d) None of the above

(iv) The initial step involved in the IC fabrication is
(a) Metallization (b) Ion implantation
(c) Oxidation (d) Silicon wafer preparation

(v) A clean room is controlled environment, where
(a) products are manufactured (b) products are stored
(c) products are displayed (d) none of these

(vi) Both gate and field oxides, are generally grown by the process of
(a) Electrochemical anodization (b) Plasma-enhanced CVD
(c) Thermal oxidation (d) None of these

(vii) Quantum device killing defects size are
(a) Less than 80 Angstrom (b) Less than 200 Angstrom
(c) More than 500 Angstrom (d) none of these

(viii) Rapid thermal annealing is required after ion implantation to:
(a) Reduce the damage in the crystal owing to nuclear energy loss
(b) Reduce the damage in the crystal owing to electronic energy loss

(c) Increase the projected range
(d) Decrease the projected straggle

(ix) Photoresist layer is formed using
(a) high sensitive polymer (b) light sensitive polymer
(c) polysilicon (d) silicon di oxide

(x) Which of the following processes is used to form a deep junction?
(a) Ion implantation (b) Diffusion
(c) Etching (d) Oxidation.

Group- B

2. (a) Critically design a clean room for VLSI fabrication, with the related parameters. [(CO1) (Create/HOCQ)]
(b) Compare the size of bacteria and virus that cause killing defects in the 16K & 64DRAM chips. [(CO1) (Understand/LOCQ)]
(c) Critically detect the reasons, why Photolithography is preferred to be done in a"Class-10" clean room and in yellow light? [(CO1)(Evaluate/HOCQ)]

6 + 3 + 3 = 12

3. (a) Explain that the Reynold number is important for epitaxial growth? [(CO2) (Remember/LOCQ)]
(b) Critically prove that the oxide growth rate is linear parabolic in thermal oxidation. [(CO2) (Evaluate/HOCQ)]
(c) Outline with necessary attributes that "Larger the crystal, smaller the pull rate". [(CO2)(Analyze/IOCQ)]

3 + 6 + 3 = 12

Group - C

4. (a) What is the Fick's 1st law & 2nd law of diffusion? [(CO4)(Remember/LOCQ)]
(b) What are the influential parameters to control the diffusion rate of impurities into semiconductor Lattice? [(CO4) (Analyze/IOCQ)]
(c) Obtain an expression for the oxide thickness 'x' in thermal oxidation and prove that the oxide growth rate is linear parabolic in thermal oxidation. [(CO2) (Evaluate /HOCQ)]

(3 + 3) + 6 = 12

5. (a) A boron doped crystal is measured at its seed end with a four point probe of spacing 1mm. The (v/i) reading is 10 ohms. Consider the solid concentration $C_s=2\times10^{15}$ atoms/cm^3 and the segregation coefficient is 0.8 and the expected reading of fraction of the melt solidified is 0.95. What is the seed end doping? [(CO4) (Understand/LOCQ)]
(b) Explain the advantages of thermal oxidation? [(CO2) (Understand/LOCQ)]
(c) Outline the attributes of transverse straggle with necessary diagram. [(CO4)(Analyze/IOCQ)]

4 + 3 + 5 = 12

Group - D

6. (a) Illustrate the process of electron beam lithographic system. [(CO3) (Understand/LOCQ)]
   (b) Outline the major constituents of a Photo-resist and their functions. [(CO3) (Analyze/IOCQ)]
   (c) Considering the pros and cons of CVD or PECVD detect the better process for Graphene synthesis. [(CO2)(Evaluate/HOCQ)]

5 + 4 + 3 = 12

7. (a) What is wet chemical etching? What are the characteristics of an ideal etchant used for wet chemical etching? [(CO2) (Remember/LOCQ)]
   (b) In Optical lithography, what parameter fundamentally determines the minimum resolvable feature size? Explain your answer briefly. [(CO3) (Analyze/IOCQ)]

(2 + 4) + 6 = 12

Group - E

8. (a) Outline the process of "LOCOS". [(CO5) (Analyze/IOCQ)]
   (b) If you critically observed the LOCOS it will be observed that the "Bird's Beak" will be constructed, how it can be minimized. [(CO5) (Evaluate/HOCQ)]

6 + 6 = 12

9. (a) Explain the process sequence needed for an n channel MOSFET fabrication. [(CO4) (Remember/LOCQ)]
   (b) Discuss the SOI fabrication technique. [(CO6) (Analyze/IOCQ)]
   (c) What is self aligned gate? [(CO5)(Understand/LOCQ)

6 + 3 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	37.5%	31.25%	31.25%

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn clean room concepts
2. Students will learn individual fabrication steps
3. Students will learn Pattern Transfer to Si from Mask using Lithography
4. Student will learn semiconductor doping techniques
5. Student will learn planner MOSFET fabrication process
6. Student will learn SOI fabrication Technology

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
VLSI	https://classroom.google.com/u/0/w/NDEwMDY5NzIwNzA3/tc/NDc0ODUzMTMxNjkx