M.TECH/VLSI/1ST SEM/VLSI 5142/2021

MODELLING OF VLSI DEVICE
(VLSI 5142)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A reverse bias applied to a diode will
(a) raise the potential barrier
(b) lower the potential barrier
(c) raise the potential barrier and increase the depletion width
(d) raise the potential barrier and decrease the depletion width

(ii) Input impedance of a practical MOSFET is
(a) very high (b) very low
(c) infinite (d) zero

(iii) The dominant current in a MOSFET operating in the strong inversion region is due to
(a) drift
(b) diffusion
(c) both drift and diffusion
(d) leakage current of drain source pn-junctions

(iv) Flat band voltage is determined by
(a) intrinsic Fermi level difference
(b) quasi Fermi level difference
(c) electron affinity
(d) metal-semiconductor work function difference, oxide and interface charge densities

(v) Pao-Sah drain current model considers
(a) drift current transport mechanism
(b) diffusion current transport mechanism
(c) both drift and diffusion current transport mechanisms
(d) some assumptions for transport mechanism

(vi) Velocity saturation of carriers in a short channel MOSFET causes the drain current to saturate at
(a) the same V_{ds} (b) a lower V_{ds}
(c) a higher V_{ds} (d) the threshold voltage

(vii) The MOSFET in saturation behaves like a
(a) constant current source (b) diode
(c) inductor (d) capacitor

(viii) The effective channel length of a MOSFET in saturation decreases with increase in
(a) gate voltage (b) drain voltage
(c) source voltage (d) substrate voltage

(ix) The MOSFET in its linear region of operation behaves like a
(a) resistor (b) capacitor
(c) inductor (d) diode

(x) Application of substrate bias causes the threshold voltage of a MOSFET to
(a) decrease (b) increase
(c) remain the same (d) become zero

Group - B

2. (a) Explain the cause of the appearance of a built-in-electric field in a pn-junction. [(CO1) (Understand/LOCQ)]
(b) Draw the energy band diagrams of a pn junction under forward bias and reverse bias conditions. [(CO1) (Understand/LOCQ)]
(c) Derive the expression for the total current density in a semiconductor when an electric field is applied in addition to carrier concentration gradients for both electrons and holes. [(CO1)(Apply/IOCQ)]

2 + 4 + 6 = 12

3. (a) Using appropriate energy band diagrams show how the diffusion and drift current change in a pn-junction under forward and reverse bias. [(CO1) (Apply/IOCQ)]
(b) Illustrate with a suitable schematic, the parasitic resistances in a typical modern n-p-n transistor.[(CO1)(Apply/IOCQ)]

6 + 6 = 12

Group - C

4. (a) Draw the energy band diagram of an n-MOS when a negative gate voltage is applied. [(CO2) (Remember/LOCQ)]
(b) Obtain an expression for the body factor of a MOSFET in terms of the permittivity of the semiconductor, electronic charge and doping concentration. [(CO2) (Apply/IOCQ)]

(c) Derive expressions for the threshold voltage of a MOSFET to show its dependence on its body factor. [(CO2)(Create/HOCQ)]

3 + 3 + 6 = 12

5. (a) Derive the drain current expression of a long channel MOSFET and explain the different regions of its I-V characteristics. [(CO2) (Create/HOCQ)]
   (b) What is substrate bias effect? [(CO2)(Understand/LOCQ)]
   (c) Show the variation of the MOSFET capacitance with change of the gate-to-source voltage. [(CO3)(Apply/IOCQ)]

8 + 2 + 2 = 12

Group - D

6. (a) State the assumptions of constant field scaling theory. [(CO5) (Remember/LOCQ)]
   (b) Show the effect of full scaling on the following MOSFET parameters: gate oxide capacitance per unit area and the packing density. [(CO5) (Apply/IOCQ)]
   (c) Justify the use of constant voltage scaling in the industry. [(CO5)(Analyze/HOCQ)]

3 + 4 + 5 = 12

7. (a) Explain the origin of the subthreshold current in a short channel MOSFET. [(CO4) (Understand/LOCQ)]
   (b) What are 'hot' electrons? [(CO4) (Understand/LOCQ)]
   (c) Show how the presence of hot electrons affect the operation of a short channel MOSFET? [(CO4)(Analyze/IOCQ)]

5 + 2 + 5 = 12

Group - E

8. (a) What are compact models for MOSFETs? [(CO6) (Remember/LOCQ)]
   (b) Why is the development of compact MOSFET models necessary for circuit simulators? [(CO6) (Understand/LOCQ)]
   (c) Compare the threshold voltage- based, charge- based and surface- potential based compact models for a MOS transistor. [(CO6)(Analyse/IOCQ)]

3 + 3 + 6 = 12

9. (a) Develop the SPICE LEVEL 1 MOSFET model from the expression of the drain current. [(CO6) (Create/HOCQ)]
   (b) Draw the equivalent circuit of LEVEL 1 MOSFET model .[(CO6) (Apply/IOCQ)]
   (c) Discuss the accuracy of LEVEL 1 MOSFET model. [(CO6)(Analyse/IOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	39.1%	43.5%	17.4%

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn BJT Modeling
2. Students will learn MOSFET Operation
3. Students will learn source of various MOSFET Capacitor Components
4. Students will learn SCE (Short Channel Effect) in MOS Devices
5. Students will learn MOS Scaling concepts on Future Technologies
6. Students will learn Industry Standard Compact Modeling

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/NDIwNTAwMDQxNzA3/tc/NDY4MjgxMTYyOTQx