M.TECH/VLSI/1ST SEM/VLSI 5102/2021

EMBEDDED SYSTEMS DESIGN
(VLSI 5102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Embedded Systems are _____ systems that do specialized tasks
(a) dedicated (b) alternative
(c) talkative (d) photographic

(ii) The work by an _____, is based and preceded by action from a sensor
(a) Injector (b) Alternator
(c) Administrator (d) Actuator

(iii) The correctness of the real time system depends not only on logical results but also on the _____ range the results are produced
(a) color (b) distance
(c) time (d) appearance

(iv) The R&D cost for a new product launched is listed under _____ cost.
(a) Unit (b) NRE
(c) Capital (d) Marketing

(v) Three key technologies used for embedded systems are processor technology, technology and design technology.
(a) system (b) IC
(c) gaming (d) computer

(vi) Which is not an embedded processor?
(a) ARM 7 (b) ARM 9
(c) AMD 29050 (d) IBM 370

(vii) The number of active elements in a DRAM cell is
(a) 1 (b) 2
(c) 6 (d) 9

(viii) The logic family which takes the least power is
(a) TTL (b) RTL
(c) CMOS (d) ECL

(ix) Watchdog timers enable an embedded system to
(a) reduce overhead (b) restart in case of failure
(c) reduce unit cost (d) improve efficiency

(x) A CAN device is
(a) serial and unidirectional (b) serial and bidirectional
(c) parallel and unidirectional (d) parallel and bidirectional.

Group- B

2. (a) What is a Real Time System? What are the differences between a RTOS and a GPOS? [(CO2) (Remember/IOCQ)]
(b) In a Sequential circuit the same input pattern applied at different instant can produce separate outputs. Explain why with examples. [(CO2) (Analyze/HOCQ)]

(3 + 3) + 6 = 12

3. (a) Implement a full adder cell using a 3×8 decoder and OR gates. [(CO2)(Apply/IOCQ)]
(b) Deduce the design of a synchronous decade up counter using JK Flip Flops. Modify the circuit to down count starting from 1111. [(CO2)(Analyze/IOCQ)]

4 + 5 + 3 = 12

Group - C

4. (a) Outline the Harvard Architecture with the help of a block diagram. [(CO5)(Remember/LOCQ)]
(b) Interpret ARM Cortex 8 Instruction Fetch Decode Unit and Execute Unit. [(CO4)(Understand/LOCQ)]
(c) A 4-stage pipeline system takes 20 ns to process a sub operation in each stage. The pipeline executes 100 tasks in sequence. Evaluate the speed up ratio? [(CO3)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

5. (a) Highlight the details of instruction pipelining. [(CO5)(Remember/LOCQ)]
(b) Outline the pipeline hazards. [(CO5)(Remember/LOCQ)]
(c) Present the major differences among Superscalar, Super pipelined and VLIW approaches. [(CO5)(Apply/IOCQ)]

4 + 4 + 4 = 12

Group - D

6. (a) Catagorise the main registers and the register bank operations of 8051 Controller. With example illustrate what are SFR registers. [(CO3)(Analyze/IOCQ)]

   (b) Show the stack and stack pointer for the following program after each stack operation. Assume default stack area and register 0 is selected.

```
MOV  R6, #25h
MOV  R1, #12h
MOV  R4, #0F3h
PUSH 6
PUSH 4
PUSH 1
HLT1.
```

[(CO4)(Understand/HOCQ)]

6 + 6 = 12

7. (a) Organize the function of Distributed Interrupt Controller for ARM 11 MPCORE processors. [(CO4)(Analyze/IOCQ)]

   (b) Outline Snoop Control Unit in ARM 11. [(CO4)(Remember/LOCQ)]

   (c) Present the ARM processor architecture memory organization with the sketch of block schematic representation. [(CO4)(Apply/IOCQ)]

5 + 3 + 4 = 12

Group - E

8. (a) Categorize between SRAM and DRAM. Explain their reading and writing operations. [(CO6)(Understand/LOCQ)]

   (b) An 8-bit DAC has a resolution of 15 mV/LSB. Determine (i) Full scale output voltage V_{fs} and (ii) Output voltage when the input digital word is "0001 0010". [(CO6)(Evaluate/HOCQ)]

6 + 6 = 12

9. (a) Explain with diagram the working principle of a DRAM and a SRAM. In the preferred use as large main memory of a system DRAM is considered over SRAM. Why and how it is accommodated ? [(CO5) (Remember/IOCQ)]

   (b) Explain "bouncing" effect in a keyboard? How is it neutralized. [(CO5) (Understand/LOCQ)]

(2 + 3 + 2) + (2 + 3) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	31.25%	45.83%	22.92%

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn Embedded System Design Methodology
2. Students will learn Embedded Processor Design
3. Students will learn 8051 Micro-controller
4. Students will learn basics of PIC & ARM Micro-controller
5. Students will learn Embedded Memory Architecture and Interface
6. Students will learn I/O Device configurations and Interfacing

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/NDE4Mjc4OTQxODE1/tc/NDc0Mzc5ODIwNzkx