M.TECH/VLSI/1ST SEM/VLSI 5101/2021

DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, the number of transistor per chip gets doubled in every
(a) 12 Months (b) 18 Months (c) 24 Months (d) 6 Months

(ii) Pentium 4 chip fall under which category as shown below
(a) VLSI (b) ULSI (c) GSI (d) TSI

(iii) Value of "Lambda" in 130nm Process Node is
(a) 130nm (b) 65nm (c) 90nm (d) 100nm

(iv) For a Standard Cell Layout
(a) Width is fixed (b) Height is fixed
(c) Both Height and Width are fixed (d) None of Above

(v) Minimum Number of Transistors in CMOS logic Y = AB + CDE is
(a) 10 (b) 12 (c) 14 (d) 8

(vi) The NMOS Transistor in its linear region can be modelled as
(a) Resistance (b) Current Source
(c) Short Circuit (d) Voltage Source

(vii) With decrease of V_{DD}, the output transition delay of an CMOS inverter
(a) Increase (b) Decrease
(c) Remains Same (d) Decrease and then increase

(viii) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis

(ix) The output of Physical Design is
(a) Logical Netlist (b) Circuit Diagram (c) RTL (d) Layout

(x) 0.7 Technology scaling enables Layout area scaling of
(a) 0.75 (b) 0.45 (c) 0.49 (d) 0.65.

Group - B

2. (a) What are the various Capacitance Components of a MOS Transistor? [(CO1) (Remember/LOCQ)]
(b) How VTC of CMOS inverter will change if Width of PMOS is increased? [(CO1) (Apply/IOCQ)]
(c) For a CMOS Inverter V_{OH} = 5V, V_{OL} = 0V, V_{IH} = 3.7V, V_{IL} = 2.1V. Find the Value of NM_H and NM_L? [(CO1) (Apply/IOCQ)]

4 + 4 + 4 = 12

3. (a) Implement Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers. [(CO2) (Apply/IOCQ)]
(b) Explain the difference between "Micron based Design Rule" and "Lambda Based Design Rule"? [(CO2) (Understand/LOCQ)]
(c) Implement the schematic and Stick Diagram of 3 input NOR gate. [(CO2) (Apply/IOCQ)]

4 + 4 + 4 = 12

Group - C

4. (a) Draw Flow Diagram of VLSI Design Cycle. [(CO3) (Remember/LOCQ)]
(b) Draw Flow Diagram of Front End Design Flow. [(CO5) (Understand/LOCQ)]
(c) Write VHDL behavioural model for a Rising Edge Triggered D –Flip Flop. [(CO4) (Apply/IOCQ)]

4 + 4 + 4 = 12

5. (a) Draw VTC Curve for CMOS Inverter and show various Regions. [(CO1) (Understand/LOCQ)]
(b) Implement Dynamic Circuit topology of 6 input NOR gate. [(CO1) (Apply/IOCQ)]
(c) Implement f = A+B Boolean logic using Transmission Gate. [(CO1) (Apply/IOCQ)]

4 + 4 + 4 = 12

Group - D

6. (a) Draw flow diagram of High Level Synthesis. [(CO5) (Remember/LOCQ)]
(b) Implement the BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b $\leq$ c. [(CO5) (Evaluate/HOCQ)]
(c) Create the ROBDD Diagram and the corresponding optimized Boolean expression. [(CO5) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

7. (a) Write VHDL code of Behavioural Modelling of a 2:1 Multiplexor. [(CO4)(Apply/IOCQ)]

(b) Write VHDL code of Behavioural Modelling of a 2 Input NOR Gate. [(CO4)(Apply/IOCQ)]

(c) Explain Technology Library Mapping for Logic Synthesis. [(CO5)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Group - E

8. (a) Why CMOS Transmission gate is used instead of NMOS pass transistor logic? [(CO1) (Analyze/IOCQ)]

(b) Implement Circuit of a negative edge triggered D-Flip Flop. [(CO1) (Apply/IOCQ)]

(c) Implement Circuit of 10 input OR gate using Domino Circuit. [(CO1) (Apply/IOCQ)]

4 + 4 + 4 = 12

9. (a) Draw Flow Diagram of Physical Layout Automation. [(CO6) (Remember/LOCQ)]

(b) For below Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
Terminal Connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2). [(CO6) (Apply/IOCQ)]

(c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm. [(CO6) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	29.2%	58.3%	12.5%

Course Outcome (CO):

After the completion of the course students will be able to
CO1. Students will learn CMOS Circuit used in Digital VLSI Domain
CO2. Students will learn Physical Layout Design of CMOS Standard Cell
CO3. Students will learn Digital VLSI Design Methodology
CO4. Students will learn HDL coding
CO5. Students will learn EDA High Level and Logic Level Synthesis Algorithms
CO6. Students will learn EDA Physical Place and Route Automation Algorithms

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
VLSI	https://classroom.google.com/c/NDE3NTE0MjU4MDIw/a/NDY4MDAyMzQ1MTYw/details