DIGITAL LOGIC
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) If (24 + 17) = 40 then the base of the numbers is
(a) 5 (b) 6 (c) 9 (d) 11

(ii) If a function is shown as F(A, B, C, D) =Σ (1,2,4,5,8,9,10,11,15), then its compliments F' is given by.
(a) F'=π(1,2,4,5,8,9,10,11,15) (b) F'=Σ (1,2,4,5,8,9,10,11,15)
(c) F'= π(0,3,6,7,12,13,14) (d) F' =Σ(0,3,6,7,8,9,10,11,15)

(iii) With respect to the input lines of a decoder, each of the output lines represents a corresponding
(a) Voltage Line (b) Maxterm
(c) Tagged Wire (d) Minterm

(iv) The logic family using the minimum power is
(a) CMOS (b) RTL
(c) TTL (d) ECL

(v) The S R flip flop goes to an indeterminate state when both its output Q and Q' are
(a) Unequal (b) Equal
(c) Undefined (d) Clipped

(vi) If the J and K inputs are shorted then the JK flip flop behaves as a
(a) SR FF (b) D FF
(c) T FF (d) JK Master Slave FF

(vii) The BCD adder adds another constant decimal value of ____ after each 4 bit addition based on conditions
(a) 4 (b) 5
(c) 6 (d) 7

(viii) A memory system uses refresh cycle to restore its contents, then type of memory the system is using is
(a) SRAM (b) DRAM (c) EEPROM (d) USB

(ix) A Decoder with an enable input represents a functional
(a) Encoder (b) Comparator
(c) Demultiplexer (d) Multiplexer

(x) Hexadecimal equivalent of the Octal number (775737264.75) is
(a) FBBF.F4 (b) 7F867FC.E3
(c) 65DE7.74 (d) 7F7BEB4.F4

Group - B

2. (a) The main stairway in a flat building has three switches to individually control the lights (switch on/off). Switch A is located at the top of the stairs, switch B is located halfway up the stairs and switch C is positioned at the bottom of the stairs. Design a logic network to control the lights on the staircase from each switch position. [(CO1) (Evaluate /HOCQ)]
(b) Given AB' + A'B = C show that AC' + A'C = B. [(CO1) (Understand /IOCQ)]

7 + 5 = 12

3. (a) Simplify using K-map in SOP form.
f(A,B,C,D) =Σ (1,2,4,5,9,10) + Σ d(6,7,8,13) (d=don't care).
[(CO1) (Analyze /IOCQ)]
(b) Determine the canonical sum-of-products representations of the function
f(x,y,z) = z + (x' + y) (x + y'). [(CO1) (Understand/LOCQ)]

6 + 6 = 12

Group - C

4. (a) Design a four input (D3-D0) priority encoder having priority in increasing order of sequence. Input D0 having the lowest, and D3 the highest priority.
[(CO1) (Evaluate/IOCQ)]
(b) Design a 4 input carry look ahead adder. Show the logic for carry propagation, carry generation, and the look ahead circuit. [(CO1) (Remember/LOCQ)]

6 + 6 = 12

5. (a) A 8 to 1 MUX is used to implement a function F(A,B,C,D). It has inputs A, B, C connected to selection lines S2, S1, and S0. The data inputs I0 to I7 are as follows. I0=I1=I5=D, I2=D', I6=I7=1, I3=I4=0. Determine the function F(A,B,C,D).
[(CO1) (Evaluate/LOCQ)]
(b) Design a single stage BCD adder and explain why addition of six is necessary?
[(CO1) (Understand/LOCQ)]
(c) Design a one bit Full adder using a 3 to 8 decoder and OR gates.
[(CO1)(Remember/IOCQ)]

4 + 5 + 3 = 12

Group - D

6. (a) Design a clocked SR Flip flop with NOR gates and show its characteristic table . Add logic to convert it to a D flip flop. [(CO2) (Understand/HOCQ)]
   (b) Explain the working principles of a Master Slave J - K flip flop and explain with reasons why it is used. [(CO2) (Remember/IOCQ)]

6 + 6 = 12

7. (a) A sequential circuit has two D flip flops A and B, two inputs x, and y, and one output z. The flip flop input equations and the circuit output are as follows:
   DA = x'y + xA
   DB = x'B + xA
   z = B
   (i) Draw the logic diagram of the circuit
   (ii) Tabulate the state table. [(CO3) (Evaluate/IOCQ)]
   (b) Convert a J-K flip flop to a T flop. [(CO2) (Understand/LOCQ)]

8 + 4 = 12

Group - E

8. (a) Explain with a schematic the working principle of a 1 bit SRAM and a DRAM and compare their relative merits and demerits. [(CO4) (Remember/HOCQ)]
   (b) A combinational circuit is described by the following functions
   F1 (A,B, C) = Σ (3, 5, 6, 7)
   F2 (A, B, C) = Σ (0, 2, 4, 7) Implement the circuit with PLA having three inputs four product terms and two outputs after simplification.
   [(CO4) (Analyze/HOCQ)]

6 + 6 = 12

9. (a) Describe a CMOS inverter circuit and discuss its advantage over nMOS and pMOS circuits using Vout versus Vin map. [(CO5) (Evaluate/IOCQ)]
   (b) In the CMOS inverter what are the transient capacitance effect causing switching delay. [(CO5) (Understand/LOCQ)]
   (c) Show the diagram of CMOS NAND2 gate. [(CO6) (Remember/IOCQ)]

5 + 5 + 2 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33.33%	44.44%	22.22%

Course Outcome (CO):

After the completion of the course students will be able to

1. Learn Binary Number system, and logic design using combinational gates.
2. Design applications of Sequential Circuits.
3. Design Finite State Machines.

4. Learn Memory classifications.
5. Learn basics of CMOS logic.
6. Learn various digital component design as used in VLSI applications

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
CSBS	https://classroom.google.com/u/0/w/NDA1Mzc1ODcwOTQw/tc/MjI3ODg5Njg5Njc2
CSE - A	https://classroom.google.com/w/NDE3Mjk2MzQ4NDE1/tc/NDc1MTQ0MDYzNzcy
CSE - B	https://classroom.google.com/w/NDA1MjQ2ODA2MDYw/tc/NDc1MTYyOTkzMzg4
CSE - C	https://classroom.google.com/c/NDYzODM1NzI2MTM3/a/NDczODM0NDc5OTAw/details
BACKLOG	https://classroom.google.com/c/NDA1Mzc1ODcwOTQw?cjc=qsochur