B.TECH/IT/3RD SEM/INFO 2101(BACKLOG)/2021

DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The base of the number system for the addition operation 24 + 14 = 41 to be true is
(a) 8 (b) 5 (c) 7 (d) 6

(ii) Which one of the following is an invalid state in 8-4-2-1 binary coded decimal counter?
(a) 1000 (b) 1001 (c) 0011 (d) 1100

(iii) Which of the following logic family has highest noise margin?
(a) TTL (b) CMOS (c) RTL (d) ECL.

(iv) How many select lines are required for a 1024:1 MUX?
(a) 65 (b) 10 (c) 128 (d)256.

(v) How many flip-flops are required to construct a decade counter?
(a) 4 (b) 8 (c) 5 (d) 10.

(vi) Internal propagation delay of asynchronous counter is removed by
(a) ripple counter (b) ring counter
(c) modulus counter (d) synchronous counter

(vii) The code used for labeling the cells of k-map is :
(a) Gray code (b) Octal code
(c) BCD (d) Hexadecimal

(viii) Data distributers are basically same as
(a) decoder (b) de-multiplexer
(c) multiplexer (d) priority encoder.

(ix) The main difference between a register and a counter is as follows.
(a) A register has no specific sequence of states
(b) A counter has no specific sequence of states
(c) A register has capability to store one bit of information but counter can store n bits.
(d) None of the above.

(x) The function AB'C + A'BC + ABC' + A'B'C + AB'C' is equivalent to
(a) AC' + AB + A'C (b) AB' + AC' + A'C
(c) A'B + AC' + AB' (d) A'B + AC + AB'.

Group–B

2. (a) Minimize the following expression using Boolean algebra:
(i) f = AB' C+ B + BD' + ABD' + A'C
(ii) f = AB[AC + (B + C')D] [(CO2) (Apply/IOCQ)]
(b) What are don't care combinations? [(CO2) (Remember/LOCQ)]
(c) Minimize the following switching function to the simplest possible POS forms:
F(A, B, C, D)= Σm(1,4,7,10,13) +Σd(5,14,15).
where d denotes don't care condition. [(CO3) (Apply/IOCQ)]

(2 + 3) + 2 + 5 = 12

3. (a) State DeMorgan's theorem [(CO2) (Remember/LOCQ)]
(b) Design a logic circuit to convert binary code y1 y2 y3 to gray code.
[(CO4) (Apply/IOCQ)]

4 + 8 = 12

Group - C

4. (a) Design a SR flip-flop using D flip-flops. [(CO3) (Apply/IOCQ)]
(b) Implement the following logic function using 8 × 1 MUX considering D as the input and A, B, C as the selection lines: F(A, B, C, D)=AB' + BD + B' CD
[(CO1)(Apply/IOCQ)]

5 + 7 = 12

5. (a) Explain S-R flip-flop using proper logic diagram and truth table.
[(CO3) (Remember/LOCQ)]
(b) Implement the following switching function using multiplexer
F(w, x, y, z) = Σm(0, 7, 11, 15) + Σd(2, 3, 4, 13) [(CO1)(Apply/IOCQ)]

5 + 7 = 12

Group - D

6. (a) Design a mod–11 down counter using J-K flip-flops and show the output using timing diagram. [(CO5) (Apply/IOCQ)]
(b) Design a 4 – bit Parallel – in Serial – out (PISO) register. [(CO5)(Apply/IOCQ)]

7 + 5 = 12

7. Design a sequence detector that produces an output 1 whenever the sequence 10101 is detected. [(CO5) (Create/HOCQ)]

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Group – E

8. (a) Explain the operation principle of Successive Approximation type ADC with suitable diagram. [(CO6) (Analyze/IOCQ)]
   (b) Mention and compare the different logic families. Why is a dual slope ADC preferred in a digital voltmeter? [(CO6) (Understand/LOCQ)]

4 + 8 = 12

9. Design an asynchronous circuit that has two inputs X1 and X2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) is received but only in that order. [(CO5)(Create/HOCQ)]

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Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	20%	55%	25%

Course Outcome (CO):

After successfully completing this course the students will be able to:

1. Assess the utility of combinational logic circuit and sequential logic circuit.
2. Develop Boolean expression applying the knowledge of logic gates and De Morgan's theorem.
3. Design logic circuits of corresponding Boolean function applying the minimization technique of Karnaugh map Quine-Mc Cluskey methods and MOD-N counter. Compare between different types of Flip Flops.
4. Apply their knowledge of number system to convert a number of any given base to another number of required base.
5. Describe different types of counters such as Ring Counter, Jhonson counter.
6. Explain A/D and D/A conversion techniques.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
IT	https://classroom.google.com/c/NDc0ODUzNjk0OTU4/a/NDc0ODUzNjk1MDkz/details