B.TECH/EE/3RD SEM/ELEC 2102/2021

ANALOG & DIGITAL ELECTRONICS
(ELEC 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) If a square wave is applied at the input of a differentiator, the output is
(a) impulse waveform (b) square waveform
(c) triangular waveform (d) sinusoidal waveform

(ii) The output impedance of an operational amplifier should be
(a) as low as possible (b) unity
(c) as high as possible (d) infinite

(iii) If the differential gain = 1000 and CMRR = 80dB, then the common mode gain of a differential amplifier is
(a) 0.1 (b) 10^8 (c) 0.08 (d) 12.5

(iv) A Schmitt trigger circuit generates
(a) triangular waveform (b) sinusoidal waveform
(c) square waveform (d) sawtooth waveform

(v) The other name of voltage follower is
(a) Inverting amplifier (b) Differential amplifier
(c) Non-inverting amplifier (d) Unity gain amplifier

(vi) Which of the following is a weighted code?
(a) 2421 (b) Excess-3 (c) Gray (d) All of the above

(vii) Which of the following is not a valid rule in Boolean algebra
(a) A+1=1 (b) A+0= 0 (c) $A \cdot A = A$ (d) $A \cdot 0 = 0$

(viii) A 4-bit parallel adder can add
(a) two 4-bit binary number (b) two 2-bit binary number
(c) four bits at a time (d) four bits in sequence

(ix) The minimum number of NAND gates required to construct an XOR gate is
(a) 3 (b) 4 (c) 5 (d) 8.

(x) A feature that distinguishes the J-K flip-flop from the S-R flip flop is the
(a) toggle condition (b) preset input
(c) type of clock (d) clear input

Group- B

2. (a) Draw and explain the transfer characteristics of an inverting amplifier using an operational amplifier. [(CO1)(Remember/LOCQ)]

(b) The transistor circuit shown in Fig. 1 uses a silicon transistor with VBE = 0.7V, IC ≈ IE and a dc current gain of 100. Determine the value of Vo.
[(CO1) (Analyze/LOCQ)]

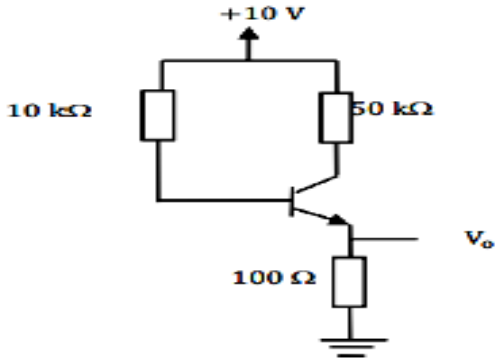

Fig. 1

(c) Design a circuit using one operational amplifier to obtain an output voltage Vout = V1 - 3V2 where V1and V2 are the input voltages. [(CO1)(Create/HOCQ)]

3 + 5 + 4 = 12

3. (a) Explain the working principle of a precision rectifier using an operational amplifier with the help of a neat circuit diagram and waveforms.
[(CO2) (Remember/LOCQ)]

(b) Model the linear differential equation using minimum number of operational amplifier: $2\frac{d^2y}{dt^2} + \frac{dy}{dt} + y = 1$. [(CO2) (Apply/IOCQ)]

(c) Determine the upper threshold voltage, lower threshold voltage and hysteresis voltage for the Schmitt trigger circuit shown in Fig. 2. Assume $R_1 = R_2 = 10k\Omega$, V_{in}(p-p) = 20V sine wave, $V_{sat} = \pm 12V$ and $V_R = 5V$. [(CO2) (Evaluate/HOCQ)]

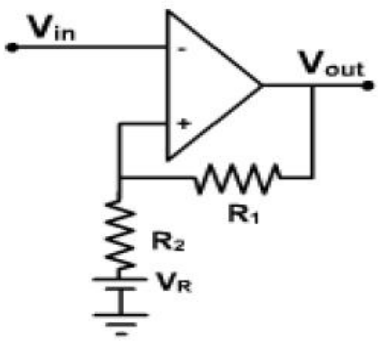

Fig.2

3 + 5 + 4 = 12

Group - C

4. (a) Compare Hartley and Colpitts oscillator. [(CO3) (Remember/LOCQ)]
   (b) Derive the expression of oscillation frequency for the Wien bridge oscillator using an operational amplifier. [(CO3) (Apply/IOCQ)]
   (c) Justify the following statement : "RC phase shift oscillator using an operational amplifier cannot be realised with only two stages in the feedback circuit." [(CO3) (Evaluate/HOCQ)]

2 + 6 + 4 = 12

5. (a) What is the nature of the trigger pulse applied in the circuit of a monostable multivibrator using an operational amplifier? [(CO3) (Understanding/LOCQ)]
   (b) Construct an astable multivibrator using a 555 timer having a duty cycle equal to 50%. [(CO3) (Apply/IOCQ)]
   (c) Design a triangular wave generator with frequency of oscillation = 2kHz and amplitude of the triangular wave Vo(p-p) = 7V. [(CO3) (Evaluate/HOCQ)]

2 + 6 + 4 = 12

Group – D

6. (a) Define D Morgan's Theorem of boolean algebra. [(CO4) (Remember/LOCQ)]
   (b) Apply the knowledge of K map to simplify the following Boolean function and implement it using suitable logic gates:
   $F(A,B,C,D) = \sum_m (0,1,2,8,10,11,14,15) + \sum_d (3,13)$. [(CO4) (Apply/IOCQ)]
   (c) Realize EX-OR and EX-NOR gates using NAND gates only. [(CO4)(Create/HOCQ)]

3 + 5 + 4 =12

7. (a) Discuss briefly about 2 lint to 4 line decoder. [(CO5) (Understand /LOCQ)]
   (b) Sketch and explain the functional diagram and write down the truth table of a 1:4 demultiplexer. [(CO5) (Apply/IOCQ)]
   (c) Design a single bit comparator, which can compare A=B, A>B and A<B. [(CO5)(Create/IOCQ)]

4 + 5 + 3 = 12

Group - E

8. (a) State the difference between asynchronous and synchronous counter. [(CO6) (Remember/LOCQ)]
   (b) Demonstrate how a JK flip flop can be used as a frequency divider circuit. [(CO6) (Apply/IOCQ)]
   (c) Design a SR flip flop using JK flip flop. [(CO6)(Create/HOCQ)]

4 + 5 + 3 = 12

9. (a) Explain the working of a 4 bit asynchronous up counter with necessary diagrams. [(CO6) (Remember/LOCQ)]

(b) Design a 4 bit SISO shift register and explain its working principle. [(CO6)(Create/HOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	28.13%	44.8%	27.08%

Course Outcome (CO):

After the completion of the course students will be able to

- Recall basic principles of diodes, transistors and OPAMPs.
- Understand basic principles of OPAMP based circuits for linear and nonlinear operations and analyze their implications.
- Acquire knowledge about different waveform generators, 555 timers, ADCs and DACs and their applications.
- Recall number systems and Boolean algebra.
- Understand Boolean algebra based realisation of logic gates and design of various arithmetic and combinational circuits.
- Design and analyze various sequential circuits like synchronous and asynchronous counters, shift registers using flip flops.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
EE	Joining Code: sywhhq3 Submission Link: https://classroom.google.com/c/NDA2NDE0NzI2MzEw/a/NDY0ODg0NTQwMzU5/details