MICROELECTRONICS AND ANALOG VLSI DESIGN
(ECEN 4111)

Time Allotted : 3 hrs   **Full Marks : 70**

Figures out of the right margin indicate full marks.

*Candidates are required to answer Group A and
<u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.*

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

    (i)   Value of "Lambda" in 180nm Process Node is
          (a) 60nm   (b) 360nm   (c) 90nm   (d) 45nm.

    (ii) Linear Region of Ideal MOS Transistor can be modelled as
          (a) Capacitance   (b) Current Source
          (c) Voltage Source   (d) Resistance.

    (iii) Short channel effects cause the threshold voltage of a MOSFET to
          (a) increase   (b) decrease   (c) remain unaltered   (d) go to zero.

    (iv) Saturation Region of Ideal MOS Transistor can be modelled as
          (a) Capacitance   (b) Current Source
          (c) Voltage Source   (d) Resistance.

    (v)   Most Popular Scaling Technique in Today's Nano Technology is
          (a) Constant Voltage Scaling   (b) Constant Field Scaling
          (c) Constant Energy Scaling   (d) Constant Charge Scaling.

    (vi) A switched capacitor circuit is associated with the disadvantage of a
          (a) overlapping clock   (b) non-overlapping clock
          (c) voltage source   (d) current source.

    (vii) The performance of a current sink/source may be improved by
          (a) reducing V_{MIN} and output resistance
          (b) reducing V_{MIN} and increasing output resistance
          (c) increasing V_{MIN} and output resistance
          (d) increasing V_{MIN} and reducing output resistance

    (viii) CMRR for a perfectly Matched Differential Amplifier Circuit is
          (a) Zero   (b) One   (c) Infinite   (d) None of above.

(ix) DIBL effects can be mitigated by
    (a) making the junction depth shallow
    (b) increasing the doping concentration
    (c) none of the above
    (d) both (a) and (b).

(x) 3D Transistor is created using below Fabrication Process
    (a) SOI   (b) FINFET
    (c) N-Well Bulk CMOS   (d) Twin Tub Bulk CMOS.

Group – B

2. (a) What is Moore's Law and what do you mean by Process Node ?
          [(CO2) (Remember/LOCQ)]
    (b) Explain enhancement type NMOS Transistor Operation.
          [(CO1) (Understand/LOCQ)]
    (c) Explain Sources of MOS Capacitance. [(CO1)(Understand/LOCQ)]

4 + 4 + 4 = 12

3. (a) What is substrate bias effect? [(CO2) (Remember/LOCQ)]
    (b) How does the threshold voltage of a MOSFET depend on substrate bias?
          [(CO3) (Understand/LOCQ)]
    (c) In the circuit shown in Fig.1, determine the output voltage if R=15 kΩ, also, calculate the maximum value of R to keep M1 operating in the saturation region. Given, V_{T0}=0.75V, γ=0.4V$^{1/2}$, surface potential at strong inversion, φ=0.6V,K=μCox=24μA/V^2. Symbols have their usual meanings.
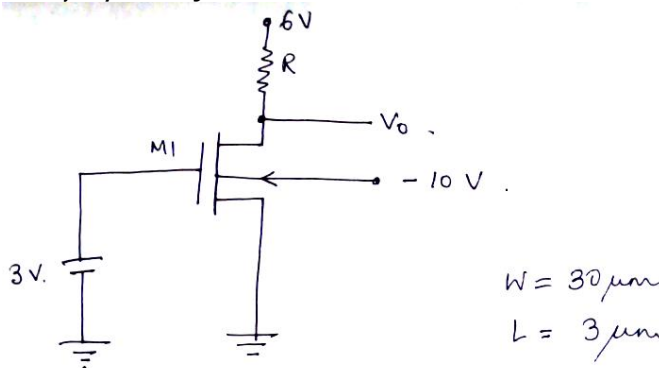

Fig.1

    [(CO4) (Evaluate/HOCQ)]

1 + 5 + 6 = 12

Group – C

4. (a) How you will use Photo Lithography using Negative Photo-resist to create N+ Diffusion in a P Type Substrate. [(CO3) (Analyze/IOCQ)]
    (b) Explain the difference between Wet Oxidation Dry Oxidation.
          [(CO3) (Analyze/IOCQ)]
    (c) Explain the difference between Lambda and Micron Rules.
          [(CO3)(Analyze/IOCQ)]

6 + 3 + 3 = 12

5. (a) Explain CMOS Fabrication flow step by step using self aligned N-Well Process Techniques. [(CO3) (Analyze/IOCQ)]
    (b) Explain Structure of FINFET Transistor.[(CO3) (Analyze/IOCQ)]
    (c) Explain Common Centroid Layout using an example. [(CO3) (Analyze/IOCQ)]

6 + 3 + 3 = 12

Group – D

6. (a) What are design Steps for Analog VLSI Flow ? [(CO4) (Remember/LOCQ)]
    (b) Explain Large Signal Models for NMOS. [(CO4) (Analyze/IOCQ)]
    (c) Evaluate Transconductance in terms of device parameters. [(CO4)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

7. (a) Obtain the high frequency equivalent circuit model of a MOSFET. [(CO4)(Apply/IOCQ)]
    (b) Why does the gain of every MOS amplifier fall off at high frequencies? [(CO4) (Understand/LOCQ)]
    (c) Show how a CMOS switch may be used to overcome the dynamic range limitations associated with a single channel MOS switch. [(CO4)(Understand/LOCQ)]

4 + 3 + 5 = 12

Group – E

8. (a) Evaluate how Basic Current Mirror Circuit can be Designed as Current Multiplier where $I_{out}/I_{in} = 4$. [(CO4)(Evaluate/HOCQ)]
    (b) Evaluate how Cascode Current Sink can increase Output Resistance. [(CO4) (Evaluate/HOCQ)]
    (c) Explain CMOS bandgap reference circuit.   [(CO4) (Analyse/IOCQ)]

4 + 4 + 4 = 12

9. (a) Explain Level Shifter Circuit of GPIO. [(CO6) (Analyse/IOCQ)]
    (b) Evaluate Differential Gain of MOS based Differential Amplifier with Load Resistance R_D and Transconductance gain of g_m of MOS Transistors as used as differential pair. [(CO5) (Evaluate/HOCQ)]
    (c) Explain Circuit of Switched Capacitor Integrator. [(CO6)(Analyse/IOCQ)]

2 + 6 + 4 = 12

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Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	38.1%	38.1%	23.8%

Course Outcome (CO):
After the completion of the course students will be able to
CO1. Understand the fundamentals of MOSFET Device Physics.

CO2. Correlate the fundamental understanding with the evolving VLSI Design Trends and Challenges.

CO3. Understand the IC Fabrication Process Flow leading to the practical realization of the scaled MOSFETs.

CO4. Analyze MOS-based analog VLSI sub-circuits and design them namely, current mirrors, voltage, and current references.

CO5. Design MOS circuits of practical importance e.g., common-source amplifiers and differential amplifiers.

CO6. Understand and apply the knowledge of analog sampled data circuits to synthesize practical circuits such as switched- capacitor filters.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission link:
ECE - A	https://classroom.google.com/w/NDA1MzgyNzY2MDM4/tc/NDY0MTg4MDUyMjk2
ECE - B	https://classroom.google.com/w/NDE3NDUwMzEzOTQx/tc/NDY0MzE3NTg5MzU1
ECE - C	https://classroom.google.com/u/0/w/NDA1MTgwNjIwNDI2/tc/NDY0MjcyNTk3OTE1