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Reliability analysis through linearity and harmonic distortion of a dual-material-gate asymmetric underlapped DGMOSFET☆

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ABSTRACT

In this paper, Harmonic Distortion (HD) of a Dual Material Gate Source Underlap Double Gate MOSFET (DMG-SU-DG) with different gate work function combination is examined. The HD occurs because of the non-linear response of the device and therefore, a detailed analysis of the HD keeping gate work function as a variable parameter ensure device reliability. The HD is analyzed in terms of few figures of merit (FOM) such as the primary component, the Second Order Harmonic Distortion (HD2), the Third order Harmonic Distortion (HD3) and lastly the Total Harmonic Distortion (THD). The parameters which are used to analysis of HD are the drain current, the transconductance and transconductance generation factor. The result of the analysis suggests a reduction of distortion as linearity increases with the decrease of the work function difference, between source side metal and that of the drain side. The circuit analysis is done using Single Stage Amplifier circuit. An extensive HD analysis of the aforementioned circuit, with the help of HD2, HD3 and THD along have also presented in this work.

1. Introduction

The present VLSI trend has got a new wing as it stormed into the nanometer realm [1,2]. Aggressive scaling of low power technologies has been the main point of concern. Though scaling gives the scientists an advantage of improved on current (I_{ON}), this miniaturization of feature size of the device leads to some serious setbacks which are known as Short Channel Effects (SCEs) [3]. For achieving an enhanced gate control over the bulk region, multi-gate devices have been proposed. Among them, the Double Gate MOSFET (DG-MOSFET) has emerged as the device of choice in contemporary research [4]. With the increasing demand of System on Chip (SoC) application, high on current is the foremost criterion. Hence, reduction in gate oxide thickness (t_{ox}) is needed.

However the reduction of t_{ox} in sub-micron technologies will cause harmful issues like gate quantum mechanical tunneling [1,5–7]. The use of high-k materials is proposed as a remedy as it increases the physical gate height. However, it offers severe scattering in the rough interfaces between oxide and bulk silicon. This problem has been mitigated by using a thin layer of SiO_2 in between the Si and the high k oxide interface, keeping the Effective Oxide Thickness (EOT) same. This well-known architecture is known as GateStack [5,8].

Non overlapping source drain structure with a lower doping in the channel region improves immunity against SCEs especially Drain Induced Barrier Lowering (DIBL) [4,9–12]. This structure is known as underlap and by offering a certain amount of excess channel length [13] it reduces the effect of DIBL [4]. However, with the increase in underlap length, the channel resistance has also increased, which in turn reduces the I_{ON}. Therefore, the underlap length should be optimized properly [8]. Even though the symmetric underlap structure provides better immunity against DIBL, it offers significantly low current. To improve the drain current while maintaining the improved immunity towards SCEs, the asymmetric underlap DG-MOSFET (A-U-DG MOSFET) structure has been proposed. Previous literatures suggest that in asymmetric cases underlaps are usually provided in the drain side for more current than its source side counterpart [14], but recently in *Sivaram* et al. [14] and [15] it has been found that with the miniaturization of the technology node under 20 nm the device consists of drain underlap shows poor DIBL performance as well as high channel length modulation for the higher drain bias. Hence, source underlap device (SU-DG MOSFET) has been proposed as a better device as far as reliability is concern.

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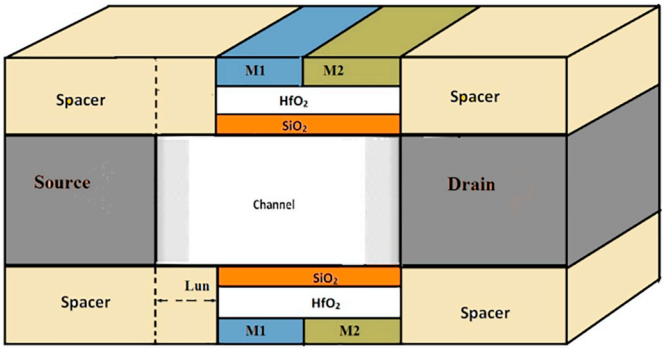

Fig. 1. DMG-SU-DG NMOSFET with metal of different work function at M1 and M2.

The further quest for better performance and reliable SCE was carried on. It was *Long* et al. [16] who introduced the scope of dual material gate (DMG) over the single material one. This architecture offers a step in the conduction band under the gate region [17,18]. The difference in work function between the two materials generates an electric field peak under the gate which reduces the possibility of hot electron effects and increases the carrier transport [19]. As a result, I_{ON} has increased. Splitting of the gate also provides screening effect, which reduces the DIBL of the device by a large extent [16].

To improve I_{ON} while increasing immunity towards short channel effects, the dual material gate is introduced to the source underlapped device and the overall effect on the performance of the device has been observed. As a result a Dual Material Gate Source Underlap Double Gate (DMG-SU-DG) MOSFET, shown in Fig. 1, with different material combination in M1 and M2 has been proposed, where M1 is the higher work function metal, and M2 is the metal with lower work function.

The device reliability has been investigated using linearity harmonic distortion (HD) analysis [20–22]. Harmonic distortion reflects the amount of non-linearity offers by the device. Hence, the study of HD will provide a clear idea of how far extends the device is reliable in radio frequency domain of application.

The simulation setup and device description has been described in Section 2. In the next two section linearity analysis has been performed. The linearity analysis is carried out on the basis of HD parameters like Second Order Harmonic Distortion (HD2), the Third order HD (HD3) and the Total HD (THD) in Section 4. In Section 5 the Harmonic distortion (HD) as well as VTC of Single Stage Amplifier Circuit has been analyzed. Finally the summarization has been done in Section 6.

2. Device description and simulation

In this study, three devices are chosen in such a way that the work function of M1 is fixed and that of M2 is variable, abiding the only constraint (i.e. work function of M1 > work function of M2), enlisted in Table 1(a).

The device parameters and the biasing voltages are chosen in accordance with International Technological Roadmap for Semiconductor (ITRS) [7] and depicted in Table 1(b) shown below of this page.

The simulation has been performed in3D simulator Synopsys TCAD using standard density gradient model to incorporate Quantum–mechanical effects [23]. A robust meshing strategy [24] is used for higher degree of accuracy reliable and accurate simulations. Drift-Diffusion models are considered for the carrier transport [25]. The Shockley-Read-Hall (SRH) recombination model is used, that considers the effect of carrier generation and recombination mechanisms with mean carrier lifetime. For scattering effect, The Lombardi Mobility Model [26] is used. The mobility equation is obtained from [27,28] respectively. The model parameters are calibrated to match the experimental results [29]. The above device structure is biased at ambient room temperature (T) of 300 K. The drain to source voltage is chosen as 0.55 V in order to extract drain current. The simulation of I_{DS}-V_{GT} has been performed to extract distortion characteristics.

Table 1(a)
Various work function combination for experiment.

M1 (eV)	M2 (eV)
5.1	4.1
5.1	4.5
5.1	4.7

The Integral Function Method (IFM) is implemented in this work to deduce the distortion parameters such as THD, HD2 and HD3 [30], which allow us to determine the Figure of Merit (FOM) of the proposed device. The effect of the materials work function on device linearity in DMG-SU-DG MOSFET on linearity has been primarily investigated in this study.

3. Linearity analysis

The built-in non-linearity in MOSFET is needed to be reduced when used in digital circuit applications. Scaling down the device dimension put a barrier to the linear nature, as the quantum mechanical effects and short channel effects arises significantly. Hence, it is required to ensure the stable device performance in RF domain due to the arrival of Third order intercept point (IP3).Also the presence of harmonics in an input signal causes the wastage of precious output power. Hence, the third order harmonic has the most negative effect as it causes the intermodulation with the adjacent frequency band. Thus, Power at IP3 (P_{IP3}) is used to express the amount of linearity as it portend the amount power of the input signal where the amplitude of 3rd order harmonic is equal to that of the fundamental one. $P_{IP3}$is measured at the maximum transconductance in the manner shown in Ref. [31].

The device having M1 = 5.1 eV, M2 = 4.7 eV provides higher value of PIP3 and hence, showing better linearity prospects, as depicted in Fig. 2. This phenomenon can be explained easily by observing the flatness of the g_m characteristics curve shown in Fig. 3. Device, with flatness in g_m shows excellent linearly feature [31].

4. Harmonic distortion analysis

Under this section the HD has been analyzed with the help of different FOMs. The effect of gate work function on the HD parameters has been analyzed in this paper. The values of which are calculated in decibel (dB) of 1 V/V scale as found in [32]. Method of IFM [30] is chosen as the extraction method of HD parameters for this work, which is based on the I_{DS}-V_{GT} plot, where V_{GT} is the gate overdrive voltage defined as $V_{GT} = V_{GS} - V_{th}$, in which V_{th} is the threshold voltage of the device. The work has been carried out with respect to gate overdrive voltage to nullify the effect of the threshold voltage variation for different devices. The amount of non-linearity associated with a device increases with the amplitude of the input signal. Therefore, the amplitude of the small ac signal (V_a) is considered to be 50 mV, and the input gate voltage is given by.

$$\mathbf{V_G = V_{GT} + V_a \sin(\omega t)} \quad (1)$$

where ω denotes angular frequency at time t. The phase angle, ωt varies from 0 to 2π. HD parameters are analyzed based on the simplified expression presented in Ref. [33].

A. Effect of different work function combination on HD2

In this portion the effect of work function on HD2 has been investigated. The 2nd order HD has been scrutinized with respect to V_{GT} and g_m/I_D. The distortion is calculated with the help of IFM methods as

Table 1(b)
Device parameters of DMG-SU-DG MOSFET.

Device parameters	Gate length (L_g)	Underlap length (L_{un})	Effective oxide thickness (EOT)		Silicon body thickness	Permittivity of spacer	Doping of source/drain region (n^+)	Doping at channel region	Gate height	Width
			Thickness of SiO_2	Thickness of HfO_2						
Values	18 nm	23 nm	0.9nm (EOT)		16 nm	7.5	10^{20} cm^{-3}	10^{16} cm^{-3}	9.1 nm	1 μm
			0.45 nm	2.89 nm						

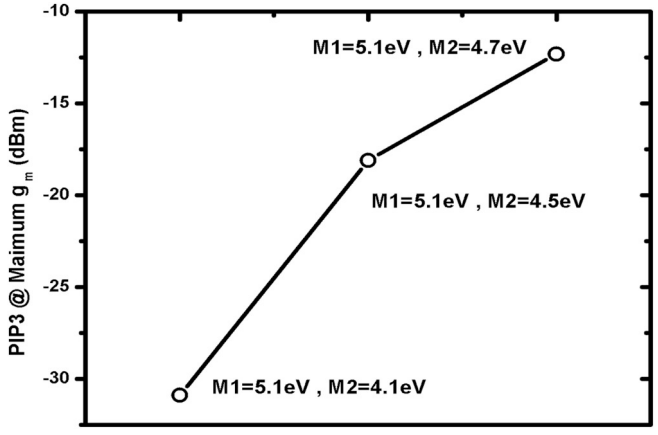

Fig. 2. Input power at IP3 of DMG-SU-DG NMOSFET at maximum g_m point for different work function combination.

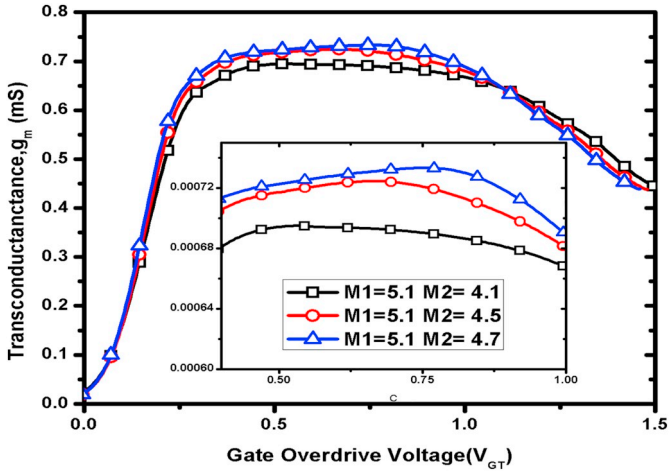

Fig. 3. g_m vs V_{GT} of DMG-SU-DG NMOSFET with materials having different work-function combination at V_{DS} = 0.82 V.

mentioned earlier. To analyze the HD2 properly with the transconductance of the device, a simple equation is provided by considering a small V_a value as mentioned in.

$$HD2 = \frac{1}{2} * V_a * \frac{1}{2 * g_m} * \frac{dg_m}{dV_{GT}} \tag{2}$$

It can be inferred from Figs. 3 and 4 that the position of the negative peak of HD2 for a device appeared at the gate voltage of maximum g_m for that particular device. Similar trend follows by the HD2 curve with g_m/I_D. As shown in Fig. 6 the sequence of the peaks of HD2 follows the peaks of g_m curve at Fig. 5. It is observed that the device with the highest g_m value shows the lowest peak in HD2 curve, which consolidate the inverse relation of g_m with HD2.

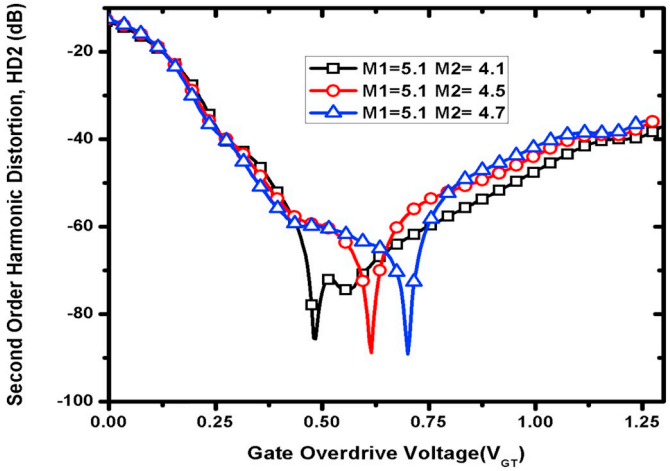

Fig. 4. HD2 with respect to V_{GT} of DMG-SU-DG NMOSFET with materials having different work-function combination.

According to the following equations,

$$g_m = \frac{dI_{ds}}{dV_{GT}} = \mu_{eff} * \frac{W}{L_{eff}} * (Q_s - Q_d) \tag{3}$$

$$\frac{dg_m}{dV_{GT}} = \frac{d^2 I_{ds}}{dV_{GT}^2} = \mu_{eff} * \frac{W}{L_{eff}} * \frac{\partial(Q_s - Q_d)}{\partial V_{GT}} \tag{4}$$

where W is the width of the device, μ_{eff} is the mobility of the carrier, Q_s and Q_d be the inversion charge in source and drain region respectively. The difference between Q_s and Q_d increases with the increase in work function of the drain side, keeping the source side fixed. Hence, device with M1 = 5.1 eV and M2 = 4.7 eV provides maximum difference of inversion charge depicted in Fig. 11, which results in maximum g_m. Therefore, according to the Eq. (2), the lowest value of HD2 or minimum distortion has been attained by the aforementioned device.

With increase in gate bias, the difference between inversion charge of source and drain region is reduced, and eventually becoming negligible. Therefore, the slope of the g_m is no longer affecting the HD2 curve. Hence, HD2 behaviour of the device is mostly dominated by g_m for higher gate voltage and lower g_m/I_D, shown in Figs. 5 and 6. However, at lower V_{GT}, the effect of increased g_m is compensated by $\frac{dg_m}{dV_{GT}}$. The increase in $\frac{dg_m}{dV_{GT}}$ for higher M2 value, is largely depends on the μ_{eff} as mentioned in Eqs. (2) and (3). The effect of V_{GT} on mobility has been depicted in the equation below.

$$\mu_{eff} = \mu_0/(1 + \theta \cdot V_{GT}) \tag{5}$$

where, μ_0 is the low field mobility and θ is the mobility degradation factor explained extensively in [31]. It is clear from the above equation that there is a strong correlation between μ_{eff} and θ. The factors by which these two device parameters are affected rigorously are Coulomb, phonon and surface roughness dependent mobility, which is discussed vastly in the next part.

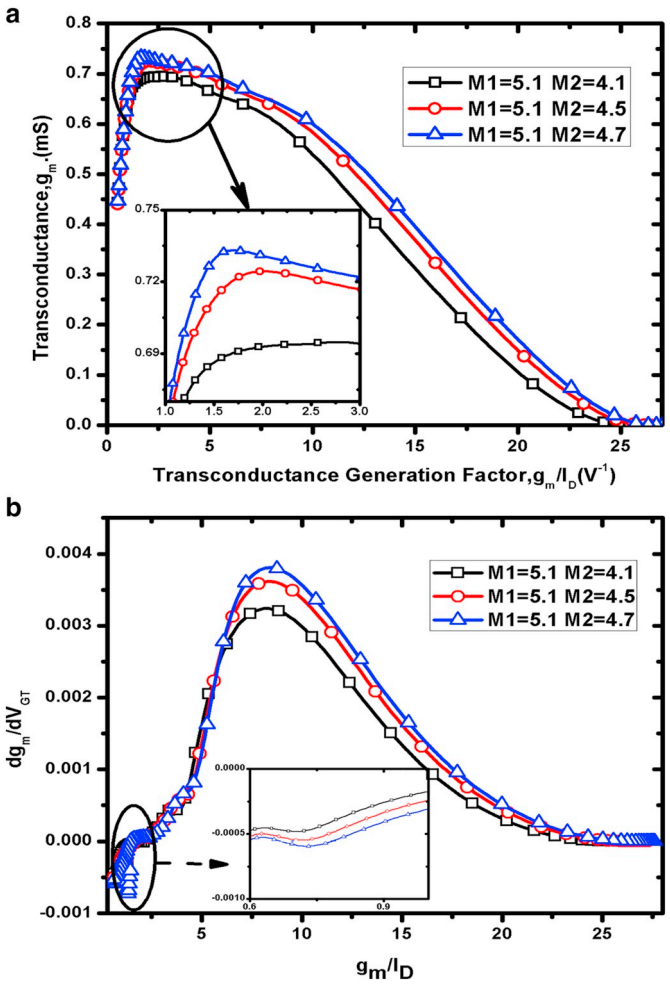

Fig. 5. a: g_m with respect to g_m/I_D of DMG-SU-DG NMOSFET with materials having different work-function combination.
b: dg_m/dV_{GT} with respect to g_m/I_D of DMG-SU-DG NMOSFET with materials having different work-function combination.

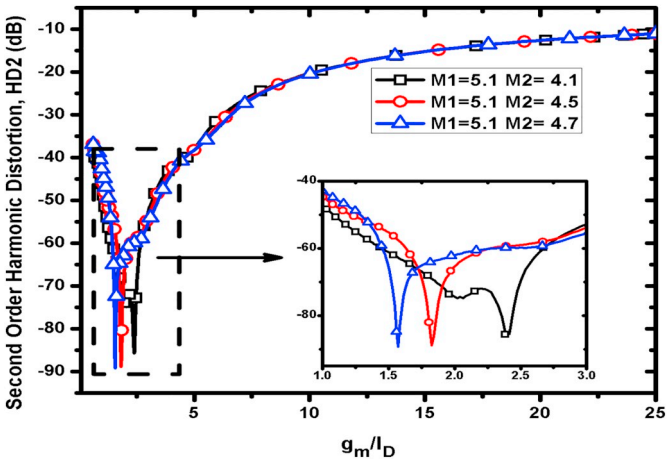

Fig. 6. HD2 with respect to g_m/I_D of DMG-SU-DG NMOSFET with materials having different work-function combination.

B. Effect of different work function combination on HD3

The expression of HD3 states that the third order harmonic distortion is directly proportional to $\frac{d^2g_m}{dV_{GT}^2}$.

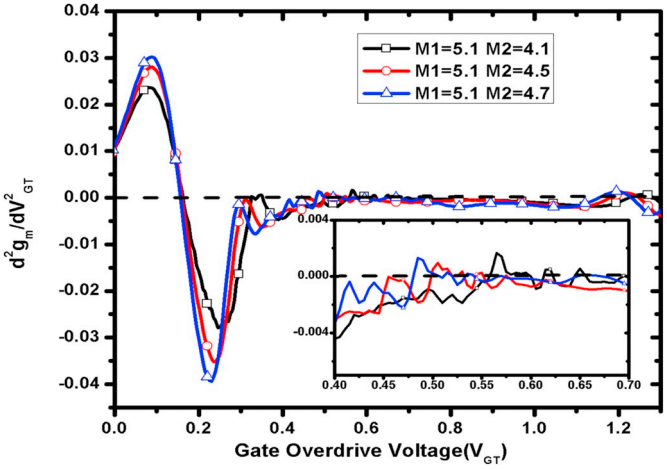

Fig. 7. $\frac{d^2g_m}{dV_{GT}^2}$ with respect to V_{GT} of DMG-SU-DG NMOSFET with materials having different work-function combination.

$$HD_3 = \frac{1}{4} * V_a^2 * \frac{1}{6 * g_m} * \frac{d^2g_m}{dV_{GT}^2} \quad (6)$$

The nature of the HD3 curve is determined by $\frac{d^2g_m}{dV_{GT}^2}$. Hence, the HD3 minima @ where $\frac{d^2g_m}{dV_{GT}^2} = 0$ [32] which is evident form Figs. 7 and 8.

The graphs show the variation of HD3 with respect to gate overdrive voltage and g_m/I_D. The plot of $\frac{d^2g_m}{dV_{GT}^2}$ has also been presented to validate the position of minima. An extensive study about the physical phenomenon behind the HD3 minima is discussed below (Fig. 9).

The mobility is restrained by underlap and channel electric fields. The electric field in the channel region depends on gate field, whereas, gate fringing fields (E_f) dominates the field in the underlap region, as shown in Fig. 10. Lowering the barrier in the underlap region by E_f boost up the carrier mobility in this region, hence effect of gate fringe-IBL (GFIBL) is observed [34]. Increase in gate voltage shifts the carrier mobility and the shift process includes coulomb scattering dependent mobility to phonon scattering dependent mobility (μ_{ph}) or from μ_{ph} to surface roughness scattering dependent mobility (μ_{sr}). Due to these, successive HD3 minima have been found as reported in [35].

The coulomb scattering is mainly due to the inversion charge in the channel region whereas phonon scattering is an energy dependent process basically occurs due to lattice vibration. The first minima is due

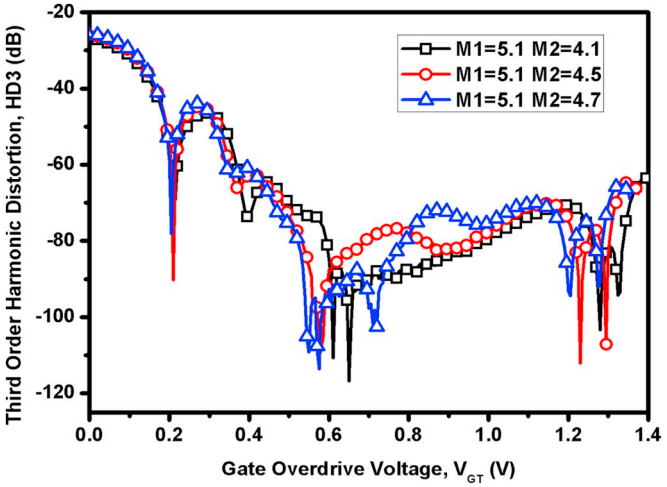

Fig. 8. HD3 with respect to V_{GT} of DMG-SU-DG NMOSFET with materials having different work-function combination.

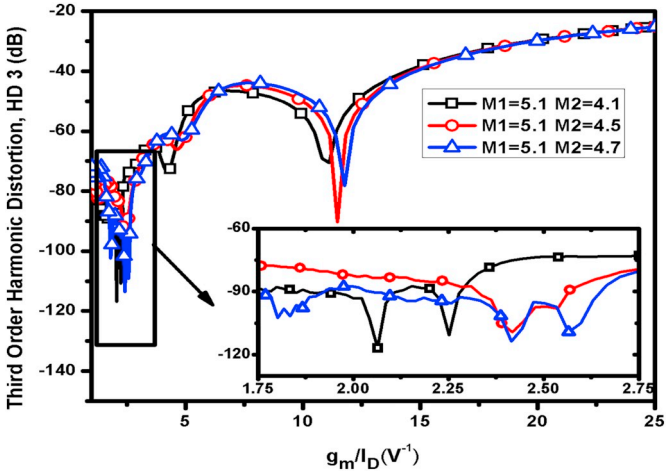

Fig. 9. HD3 with respect to g_m/I_D of DMG-SU-DG NMOSFET with materials having different work-function combination.

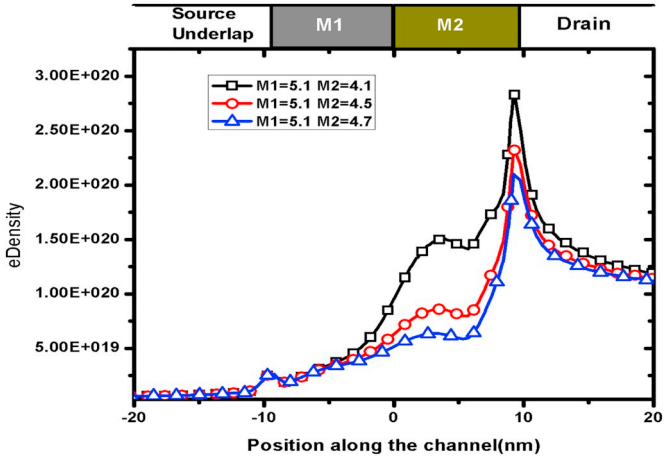

Fig. 11. Electron density (cm^{-3}) of DMG-SU-DG NMOSFET along the channel, with materials having different work-function combination at where V_{DS} = 0.82 V.

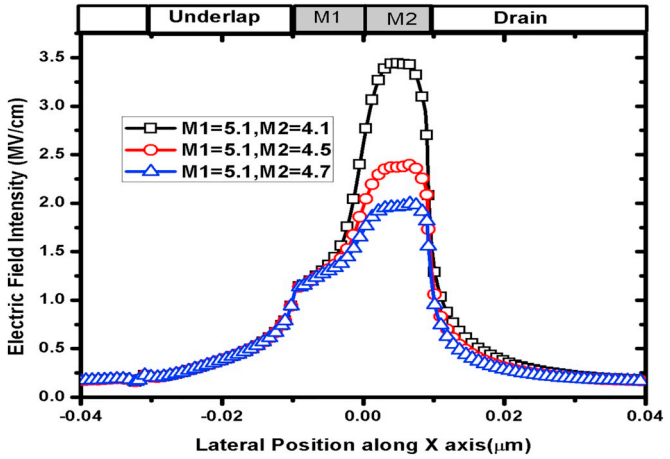

Fig. 10. Electric field of DMG-SU-DG NMOSFET along the channel, with materials having different work-function combination at V_{DS} = 0.82 V.

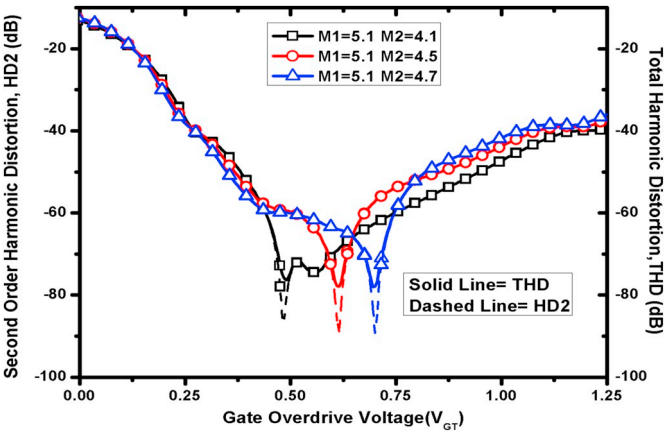

Fig. 12. THD with respect to V_{GT} of DMG-SU-DG NMOSFET with materials having different work-function combination.

to the transition from μ_{coul} to μ_{ph} in the channel region, as the nature of three devices are similar in the channel region for low gate voltage, there is no effect of Coulomb scattering due to low inversion charge and phonon scattering doesn't have much impact in the channel region, hence the minima are coincided. Therefore, linearity of the device increases subsequently. The second and third minima appear due to the μ_{coul} to μ_{ph} in the underlap region. Ideally these two minima should be overlapped but due to the asymmetric nature of the device, the effect of E_f is more on the drain side, which deviate the position of two minima. The fourth one is due to the transition of μ_{ph} to μ_{sr} in the channel region.

As the channel characteristics e.g. Si-SiO_2 interface is same for all three devices, hence the effect of phonon and surface roughness scattering are nullified in the channel region. The effects of those are treated as constant. Due to which a bunch of the fourth minima at the same gate voltage is expected. But as it can be seen, the device with M1 = 5.1 eV, M2 = 4.1 eV has attained the higher minima at higher V_{GT}. Since the correlation length for the devices considered here is identical [36], the effect of surface roughness remains constant. The inversion charge (Q_{inv}) is enhanced for the device with lower work function in drain side, resulting in delayed μ_{ph} to μ_{sr} transition [32]. Hence device with M2 = 4.1 eV has attained minima at higher V_{GT}. The positions of

Table 2
Minima of HD3 at different gate overdrive voltage (V_{GT}) (in volts) for different work function combination.

Minima of HD3 at different gate overdrive voltage (V_{GT}) in volts					
Devices	1st Minima	2nd Minima	3rd Minima	4th Minima	5th Minima
M1=5.1 eV, M2=4.1 eV	0.21	0.61	0.65	1.28	1.325
M1=5.1 eV, M2=4.5 eV	0.21	0.58	0.585	1.23	1.295
M1=5.1 eV, M2=4.7 eV	0.205	0.55	0.575	1.205	1.275

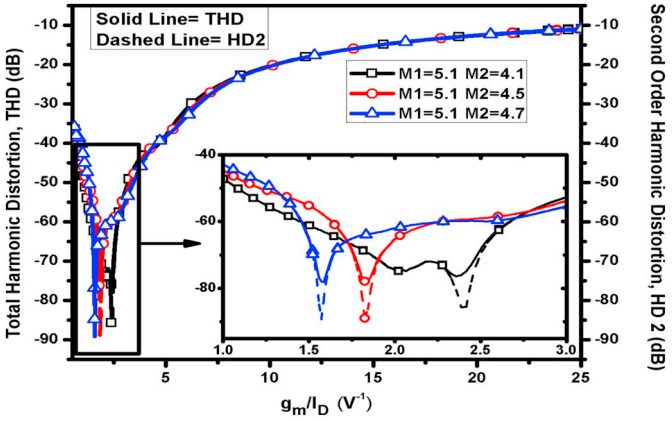

Fig. 13. THD with respect to g_m/I_D of DMG-SU-DG NMOSFET with materials having different work-function combination.

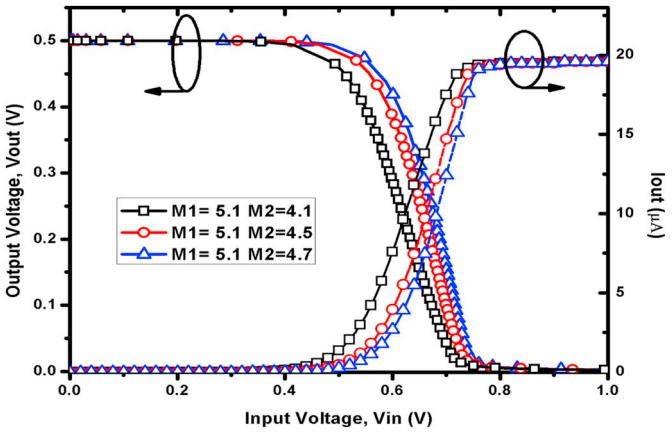

Fig. 14. Output characteristics of single stage amplifier circuit of DMG-SU-DG NMOSFET.

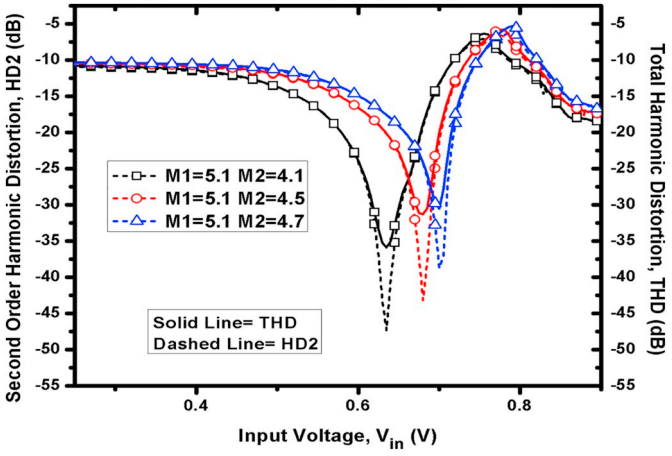

Fig. 15. HD2 and THD with respect to V_{in} of a single stage amplifier circuit with DMG-SU-DG NMOSFET.

minima are shown in Table 2.

The Q_{inv}, accumulate in the channel region, should be equal due to the same effective oxide thickness [28], but in reality different scenario have been observed. As different work function combinations are used in the gate metal, Q_{inv} accumulated in the channel region will be different, depicted in Fig. 11. Hence, with higher Q_{inv}, the device with the lowest drain side work function has provides a better charge screening,

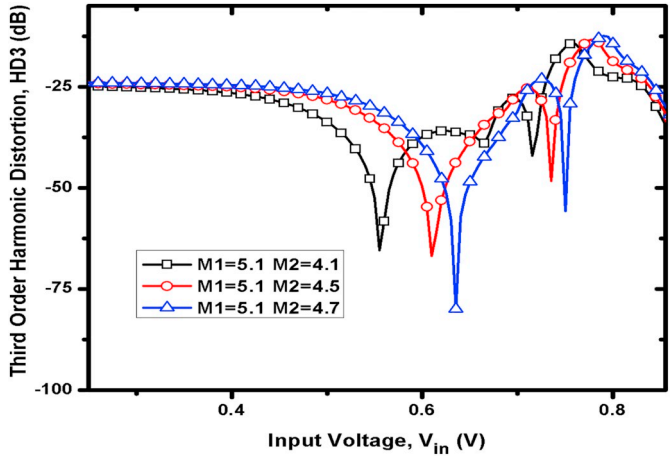

Fig. 16. HD3 with respect to V_{in} of a single stage amplifier circuit with DMG-SU-DG NMOSFET.

which resulting into increased bulk carrier mobility. Therefore high conductivity in turn reduces the HD3 values at higher V_{GT}.

C. Effect of different work function combination on THD

The total harmonic distortion (THD) is calculated by considering each and every harmonics. Though, THD is mostly influenced by HD2, HD3 has a significant role to play for even harmonics suppression.

Figs. 12 and 13 show the THD curve follows the HD2 curve except the minima point. At the minima, effect of HD2 has been conquered by HD3. Hence, THD minima have been found at a higher value than that of HD2.

5. HD performance of a single stage amplifier

In this section, a single stage amplifier circuit [37–39] is designed using the devices as the driver transistor. DC analysis has been performed with the help of output voltage and current characteristics for the aforementioned circuit, depicted in Fig. 14. It has been observed that the device with higher off current shows the sharper transition than others, in Fig. 14.

A. Effect of HD on a single stage amplifier circuit

In this section the HD performance of single stage amplifier circuit is analyzed with DMG-SU-DG as the driver MOSFET. To study the impact of HD, the prime focus has been restricted to the nature of output current with respect to the input dc voltage (V_{in}) applied to the circuit. The ac small signal, which is helpful to calculate the distortion through IFM method [28], has been superimposed on the dc value. The HD FOMs are extracted by focusing on the dynamic region. From Fig. 15, it is inferred that the THD curves follows the HD2 except the minima. The THD depicts higher minima than HD2, due to the higher value of odd harmonics. Figs. 14 and 15 have clearly explained the effect of work function on HDs. HD2 shows its minima at the voltage of maximum gain. Hence, the device with lower work function at drain side shows the minima at lower V_{in}, because the device having lower work function in the drain side, provides lower threshold voltage due to easier accumulation of inversion charge [19].

Hence, the point of maximum gain, which lies at the midpoint of dynamic region, appears much earlier for the device with lower work function in the drain side as compare to the higher one due to the early discharge of the capacitor through the driver MOSFET. The variation in current shows in Fig. 14 can be explained using HD3. There are two minima found in case of HD3, shown in Fig. 16.

The first one suggests the point where the current starts to increase significantly, whereas the second one signifies the input voltage, where the current attains its saturation value. The sequence of the minima of HD3 follows the same order as that of HD2 because of the same reason stated above.

6. Conclusion

The DMG-SU-DG NMOSFET is analyzed on the basis of Linearity performance. In this study, it is shown that the device with higher work function in drain side showcases the most linear characteristic. An extensive study of harmonic distortion with the help of HD2, HD3, THD has been done under the purview of carrier mobility and its transition. Due to the minor deficit in case of g_m, the device with lower work function in the drain side possess slightly less HD2 and THD, but on the other hand by providing high electric field in the material junction this device showcases better mobility in the channel region, results in better HD3. The harmonics of the single stage amplifier has also been analyzed, where it is evident that the device with larger difference in work functions not only reduces the circuit distortion but also the dynamic power. Moreover, shifting of g_m is towards lower V_{in}, which makes it more suitable in low power SoC application.

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