B.TECH/ECE/5TH SEM/ECEN 3104(BACKLOG)/2021

MICROPROCESSORS, MICROCONTROLLERS & SYSTEMS
(ECEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which bus is a bidirectional bus?
(a) Address bus (b) Data bus
(c) Address bus and Data bus (d) None of the above.

(ii) When an error occurs in a program and an instruction needs to be eliminated it is more convenient to substitute the eliminated instruction with
(a) HLT (b) Add 00H (c) NOP (d) RESET.

(iii) The instruction OUT cannot send data from any register other than
(a) Program Counter (b) Register B
(c) Accumulator (d) Flag register.

(iv) A register in the microprocessor that keeps track of the answer or results of any arithmetic or logic operation is the?
(a) Stack pointer (b) Program counter
(c) Instruction pointer (d) Accumulator.

(v) In 8085, TRAP is?
(a) Always maskable interrupt (b) Non-maskable interrupt
(c) Lowest priority interrupt (d) None of these.

(vi) A 4K byte memory will require
(a) 12 address lines (b) 14 address lines
(c) 10 address lines (d) 13 address lines.

(vii) The bits of the PSW Register which are responsible for selection of register banks of 8051 are
(a) PSW.3 and PSW.4 (b) PSW.3 and PSW.2
(c) PSW.3 and PSW.1 (d) PSW.3 and PSW.5

(viii) 8259 is
(a) programmable DMA controller (b) programmable interval timer
(c) programmable interrupt controller (d) DMA controller.

(ix) The number of register banks present in 8051microcontroller is
(a) 8 (b) 32 (c) 4 (d) 128.

(x) How many data lines are there in 8086 microprocessor?
(a) 16 (b) 8 (c) 20 (d) 12.

Group – B

2. (a) Explain the functions of control and status signals? [(CO2) (Remember/LOCQ)]
(b) The lower order address bus is demultiplexed to be used as data bus-Justify. [(CO2) (Analyse/IOCQ)]
(c) Draw the block diagram of a microprocessor and explain briefly the functions of each block. [(CO1) (Understand/LOCQ)]

4 + 4 + 4 = 12

3. (a) Why do we need to use tristate logic in microprocessor?
[(CO2) (Analyse/IOCQ)]
(b) Control signals are used to generate separate signals for I/O and memory operations.-Justify with diagram. [(CO2) (Analyse /IOCQ)]
(c) Explain the structure of address bus and data bus of 8085.
[(CO2) (Remember/LOCQ)]

3 + 5 + 4 = 12

Group – C

4. (a)

Memory Location	Machine Code	Instruction
2000H	3EH	MVI A, 32H
2001H	32H	

Design a timing diagram for the instruction mentioned in the above table.
[(CO2) (Create/HOCQ)]
(b) Explain the operations of BIU and EU present in 8086 processor.
[(CO4) (Remember/LOCQ)]
(c) Identify the addressing modes of the following instructions:
(i) SUB R (ii) IN 67H (iii) ANI 45H (iv) JZ 6007H (v) ORI 56H (vi) ADD M (vii) RAR (viii) DCRC. [(CO2) (Apply/IOCQ)]

4 + 4 + 4 = 12

5. (a) Compare between Push and Pop & Call and Return instructions.
[(CO3) (Analyse/IOCQ)]
(b) Five readings 56, 34, 12, 89, 23 are stored in memory locations 5005, 5006, 5007, 5008, 5009 respectively. Design a flowchart and an ALP to arrange the numbers in ascending order. [(CO3) (Create/HOCQ)]

(c) Design an ALP to enable all the interrupts of 8085. Also design another ALP to enable only RST6.5 and disable RST7.5 and RST 5.5. [(CO3) (Create/HOCQ)]

4 + 6 + 2 = 12

Group – D

6. (a) Design an ALP to generate a pulse every 100 micro second from counter 0 of Programmable Interval timer. Assume the clock frequency of the timer to be 2MHz and the address of the control register and counter 0 to be 73H and 70 respectively. [(CO5) (Create/HOCQ)]

(b) What are the commonly used priority modes of 8259A? [(CO5) (Remember/LOCQ)]

(c) 8259A requires two types of command words – Justify. [(CO5) (Analyse/IOCQ)]

6 + 2 + 4 = 12

7. (a) How does 8255 communicate with peripherals? [(CO5) (Understand/LOCQ)]

(b) Draw the block diagram of Programmable Interrupt Controller 8259. Explain the function of the control logic. [(CO5) (Remember/LOCQ)]

(c) Design a BSR control word subroutine to set bits pc7 and pc3 and reset them after 20ms. Assume the address of control register of 8255 is 53H. Consider that a delay subroutine is available. [(CO5)(Create/HOCQ)]

2 + 5 + 5 = 12

Group – E

8. (a) Draw the TMOD register of 8051. Explain the function of the mode selection bits. [(CO6) (Remember/LOCQ)]

(b) Differentiate between the instruction MOV R0, #80H and MOV R0, 80H. Write the assembly language program in 8051 microcontroller to add the numbers 56H and 95H and show manually how the CY, AC and P flags are affected. [(CO6) (Analyse/IOCQ)]

(c) Explain the interrupt system of 8051 microcontroller. [(CO6) (Remember/LOCQ)]

4 + 4 + 4 = 12

9. (a) Distinguish between polling and interrupt system of 8051. [(CO6) ((Analyse/IOCQ)]

(b) What is the advantage of register indirect addressing? [(CO6) (Analyse/IOCQ)]

(c) Compare two programs to copy the value 55H into RAM using register indirect addressing mode without and with a loop considering five memory locations. [(CO6) (Analyse/IOCQ)]

4 + 2 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	34.37%	41.66%	23.95%

Course Outcome (CO):

After the completion of the course students will be able to

1. Understand the basics of microprocessor and microcontroller with the help of previous knowledge of Digital Electronics.
2. Develop the concepts of MPU, timing and control signals I/O devices, types of BUS, etc. that form the background of this course.
3. Develop the ALP for given problems with flowchart and learn about the interrupts stack and subroutine.
4. Learn and apply the architecture of 8086 family.
5. Analyze and solve memory interfacing and I/O interfacing problems and develop idea about several peripheral devices.
6. Analyze the architecture of microcontroller 8051 with respect to I/I ports, Memory, Counters and Timers etc.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
ECE - BACKLOG	CLASS INVITE LINK: https://classroom.google.com/c/NDY0MjQyMTc4ODEz?cjc=3sisqgt
	CLASS CODE: 3sisqgt
	END SEMESTER SUBMISSION LINK: https://classroom.google.com/w/NDY0MjQyMTc4ODEz/tc/NDY0MjQzMzczNTM