B.TECH/ECE/5TH SEM/ECEN 3104/2021

MICROPROCESSORS AND MICROCONTROLLERS
(ECEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Calculate the address lines required for an 8K-byte (1024 × 8 = 8192 registers) memory chip:
(a) 11 address lines (b) 12 address lines
(c) 13 address lines (d) 14 address lines.

(ii) When an error occurs in a program and an instruction needs to be eliminated it is more convenient to substitute the eliminated instruction with
(a) HLT (b) Add 00H (c) NOP (d) RESET.

(iii) Accumulator is implicitly considered as one of the operands in all arithmetic instructions except the:
(a) AND (b) XOR and OR
(c) INR and DCR (d) None of these.

(iv) In a microprocessor, the address of the new next instruction to be executed is stored in:
(a) Stack pointer (b) Address latch
(c) Program counter (d) General purpose register.

(v) Addition of F2H and 7AH sets the flags as:
(a) CY=1, Z=0, S=0 (b) CY=1, Z=1, S=0
(c) CY=0, Z=1, S=0 (d) CY=1, Z=0, S=1

(vi) XCHG instruction of 8085 exchanges the content of:
(a) Top of stack with contents of register pair (b) BC and DE register pair
(c) HL and DE register pair (d) None of the above.

(vii) How many 16-bit registers are there in 8051?
(a) 2 (b) 3 (c) 1 (d) 0

(viii) Which of the following flag condition is used for BCD arithmetic operations in microprocessor?
(a) Sign flag (b) Zero flag
(c) Parity flag (d) Auxiliary carry flag.

(ix) The Intel 8086 microprocessor is a …… bits processor.
(a) 32 (b) 8 (c) 4 (d) 16.

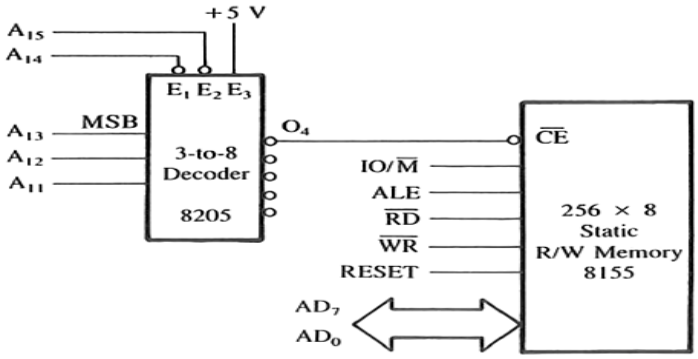
(x) The bits of the PSW Register which are responsible for selection of register banks of 8051 are:
(a) PSW.3 and PSW.4 (b) PSW.3 and PSW.2
(c) PSW.3 and PSW.1 (d) PSW.3 and PSW.5

Group – B

2. (a) Draw the flag register of 8085. Under what condition the zero and carry flag will go to the SET state? [(CO2)(Remember/LOCQ)]
(b) Why do we require the ALE pin in 8085? [(CO2)(Analyze/IOCQ)]
(c) Explain with a proper example how all the three buses and control signals work collectively to execute a memory read cycle. [(CO2)(Understand/LOCQ)]

4 + 4 + 4 = 12

3. (a) Determine the total delay for time delay using one register with the help of a proper example. [(CO2)(Analyze/IOCQ)]
(b) Analyze the decoding logic and the memory address range of the 8155 for the following diagram.



Distinguish between absolute and partial decoding. [(CO2) (Analyze/IOCQ)]
(c) If the memory chip size is 1024 x 4 bits, how many chips are required to make up 2K(2048) bytes of memory? [(CO2)(Analyze/IOCQ)]

4 + (2 + 1 + 2) + 3 = 12

Group – C

4. (a) Given the components as listed, design an interfacing circuit for memory section of 8085 to meet the following specifications:
(i) 3 to 8 decoder
(ii) 4K × 8 EPROM – address range should begin at 0000H and additional 4K memory space should be available for future expansion.
(iii) 2K × 8 CMOS R/W memory. [(CO5) (Create/HOCQ)]

(b) With the help of a proper diagram, explain the flag register for 8086 microprocessor. [(CO4)(Remember/LOCQ)]

(c) If the memory chip size is 1024x4 bits, how many chips are required to make 2K bytes of memory. [(CO5)(Analyse/IOCQ)]

6 + 4 + 2 = 12

5. (a) Design an ALP for exchanging the contents of the BC and HL register pair using PUSH and POP instructions in 8085. [(CO3) (Create/HOCQ)]

(b) Classify the interrupt structure of 8085 based on hardware and software interrupts, vectored and non-vectored interrupts. Prioritize the interrupt structure of 8085. [(CO3) (Analyze/IOCQ]

(c) What are the operations of the BIU and the EU present in 8086 microprocessor? [(CO4)(Remember/LOCQ)]

4 + (3 + 3) + 2 = 12

Group – D

6. (a) Discuss in details the interrupt operation of 8259A. [(CO5) (Remember/LOCQ)]

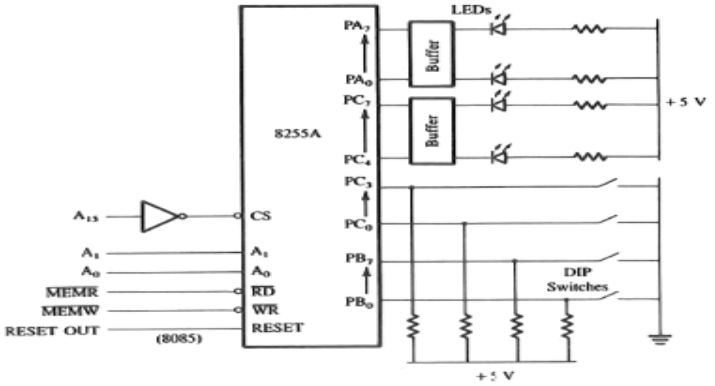
(b) Illustrate the concept of switching from the slave mode to the master mode in relation to DMA? [(CO5) (Understand/IOCQ)]

(c) Differentiate between the different modes of operation of 8254. [(CO5)(Remember/LOCQ)]

4 + 4 + 4 = 12

7. (a) What do you mean by Mode 0, Mode 1 and Mode 2 for 8255 PPI chip? [(CO5)(Remember/LOCQ)]

(b) In the following diagram for 8255 PPI,



(i) Identify the port address given in the figure.

(ii) Identify the Mode 0 control word to configure port A and port C_u as output ports and port B and port C_L as input ports. [(CO5)(Apply/HOCQ)]

(c) Discuss in details about the features of 8259A. [(CO5)(Remember/LOCQ)]

4 + (2 + 2) + 4 = 12

Group – E

8. (a) Differentiate between the instructions MOV R0, #55H and MOV R0, 55H. Write the assembly language program in 8051 microcontroller to add the numbers 56H and 95H and show manually how the CY, AC and P flags are affected. [(CO6)(Analyse/HOCQ)]

(b) Describe the program status word register of 8051 microcontroller. [(CO6) (Remember/LOCQ)]

(c) Explain the interrupt system of 8051 microcontroller. [(CO6) (Remember/LOCQ)]

6 + 2 + 4 = 12

9. (a) Distinguish between interrupt and polling in 8051 microcontroller. [(CO6) (Analyze/IOCQ)]

(b) Define the conditional and unconditional jumps present in 8051. [(CO6) (Remember/LOCQ)]

(c) Determine the contents of the PSW register after the execution of the following instructions.
MOV A, # 0BFH.
ADD A, # 1BH. [(CO6)(Evaluate/HOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	41.67%	33.33%	25%

Course Outcome (CO):

After the completion of the course students will be able to

1. Demonstrate the knowledge of Digital Electronics with learning of the microprocessor and microcontroller.
2. Develop the concepts of CPU, timing and control signals I/O devices, and various BUS structure.
3. Learn about interrupts, stack and subroutine and write ALPs for given problems with flowcharts.
4. Conceptualize the architecture of 8086 family & ARM basics along with its parallel application.
5. Understand interfacing of processor with memory and I/O devices and analyze their problems.
6. Analyze microcontroller 8051 architecture in terms of Ports, Memory, Counters and Timers.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
ECE A	https://classroom.google.com/w/NDAzNzY3MTYyNzM4/tc/NDYzODc2MzQ5NDk4
ECE B	https://classroom.google.com/w/NDA1MzUyMTkwNTQz/tc/NDY0MTc1MTEyODc2
ECE C	https://classroom.google.com/w/NDAxNjU3NDMzNTE2/tc/NDYzOTI0NDk1MTE1
Backlog	https://classroom.google.com/c/NDY0MTczOTgwMTUx?cjc=f7qmwhr