B.TECH/CSE/5TH SEM/ECEN 3106/2021

ELECTRONIC DESIGN AUTOMATION
(ECEN 3106)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) NMOS transistor switch passes
(a) Weak "zero" (b) Strong "zero"
(c) Strong "one" (d) Both (a) & (c)

(ii) Ideal Current Source has Resistance of value
(a) 0 ohm (b) Infinite
(c) 100 K ohm (d) 10 ohm

(iii) Full Custom design is preferred when
(a) Final design must have minimum area
(b) Design time is less of a factor
(c) Design is Cost sensitive
(d) All of the above.

(iv) During technology migration to next process node Lambda based design rule assumes all manufacturing dimensions scale
(a) double (b) equally (c) half (d) None of the above

(v) Memory Design is normally done using below Method
(a) Full Custom (b) Std Cell based Semi Custom
(c) FPGA (d) Gate Array.

(vi) NMOS Transistor in linear region can be modelled as
(a) Resistance (b) Current Source
(c) Open Circuit (d) Voltage Source.

(vii) With decrease of V_{DD}, the Delay of an CMOS inverter
(a) Increases (b) Decreases
(c) Remains Same (d) Decreases and then increases.

(viii) The operating regions of the transistors at the threshold voltage of *CMOS* inverter given by
(a) *NMOS* linear, *PMOS* saturation (b) *NMOS* saturation, *PMOS* linear
(c) *NMOS* linear, *PMOS* linear (d) *NMOS* saturation, PMOS saturation

(ix) Minimum Number of Transistors in CMOS logic Y = ABC + D is
(a) 12 (b) 6 (c) 14 (d) 10.

(x) Stick Diagram Represents
(a) Logic (b) Circuit
(c) Layout (d) Architecture.

Group – B

2. (a) What are various Capacitance Components of a MOS Transistor. [(CO1)(Understand/LOCQ)]
(b) Draw VTC (Voltage Transfer Curve) of CMOS Inverter and show various regions. [(CO2)(Understand/LOCQ)]
(c) For a CMOS Inverter V_{OH} = 5V, V_{OL} = 0V, V_{IH} = 3.1V, V_{IL} = 2.3V. Find the Value of NM_H and NM_L. [(CO2)(Remember/LOCQ)]

4 + 4 + 4 = 12

3. (a) Explain the differences between Full Custom Design and Std Cell based Semi Custom Design. [(CO1) (Analyze/IOCQ)]
(b) Implement schematic of CMOS gate which represents function f = (A+B+C) ! (! Means Bar). [(CO2) (Analyse/IOCQ)]
(c) Evaluate Stick Diagram of the same CMOS gate. [(CO2) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

Group – C

4. (a) Briefly discuss the standard cell based layout design method with necessary floorplan diagram. [(CO1)(Understand/LOCQ)]
(b) Implement the following logic function using *AND / OR* plane *PLA*
F1 = ab + bc + cd
F2 = a'b'd' + ae
F3 = a'c + ac' + ad' + ae' [(CO1)(Apply/IOCQ)]

6 + 6 = 12

5. (a) Solve Euler Path Algorithm for the function f =(C(A + B)) ! (! Means Bar). [(CO2) (Evaluate/HOCQ)]
(b) Evaluate Stick Diagram accordingly. [(CO2) (Evaluate/HOCQ)]
(c) Describe difference between Behavioural and Structural Model of Verilog coding using an example. [(CO5)(Analyze/IOCQ)]

4 + 6 + 2 = 12

Group – D

6. (a) Draw flow diagram of Logic Synthesis. [(CO5) (Remember/LOCQ)]
   (b) Implement BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a ≤ b≤ c [(CO5) (Evaluate/HOCQ)]
   (c) Create ROBDD Diagram for the same function f and corresponding optimized Boolean Expression. [(CO5) (Evaluate/HOCQ)]

4 + 4 + 4 = 12

7. (a) Draw Flow Diagram of Physical Layout Automation.[(CO6) (Remember/LOCQ)]
   (b) Formulate Floorplanning problem, with inputs, outputs and Objective (Cost) function. [(CO6) (Analyze/IOCQ)]
   (c) Explain Lee Algorithm of Maze Routing.[(CO6) (Analyze/IOCQ)]

4 + 4 + 4 = 12

Group – E

8. (a) Distinguish between global and detailed routing. [(CO6)(Understand/LOCQ)]
   (b) Distinguish between placement and floorplanning problem. [(CO6)(Understand/LOCQ)]
   (c) Consider Fig.1 with initial partition *A = {2,3,4}* and *B = {1,5,6}.* Apply *K-L* partitioning algorithm and compute all possible gain pairs for (*a,b*) node swapping. Evaluate the node swapping that provides maximum gain at the end of this iteration. [(CO6)(Evaluate/HOCQ)]

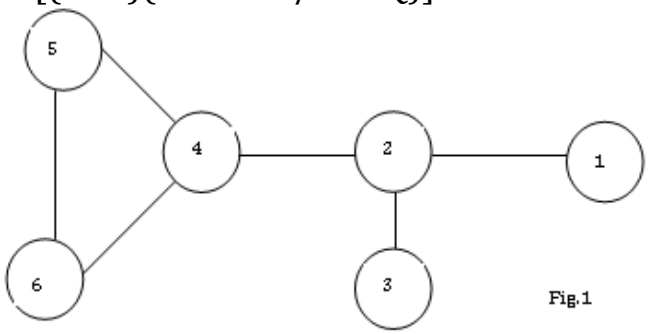

Fig.1

4 + 4 + 4 = 12

9. (a) For below Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
   Terminal Connection is as follows:
   11122563040 ----- Upper Boundary
   25055330604 ----- Lower Boundary
   0 means no Connection.
   Assume HV Layer (V = Metal 1, H = Metal 2) [(CO6) (Analyze/IOCQ)]
   (b) Evaluate Optimum Channel Routing Solution for above case using Left Edge Algorithm. [(CO6)(Evaluate/HOCQ)]
   (c) Write problem formulation of Global Routing using Steiner Tree. [(CO6)(Analyze/IOCQ)]

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	34.78%	34.78%	30.8%

Course Outcome (CO):

After the completion of the course students will be able to

CO.1. Getting exposure to VLSI Design Cycle, Process nodes and Design Challenges.
CO.2. Designing of Industry Standard CMOS Combinational Digital Gates.
CO.3. Designing of Industry Standard TG based Sequential Digital Gates.
CO.4. Learning High Level Synthesis in EDA flow.
CO.5. Learning Logic Synthesis in EDA flow and Verilog RTL.
CO.6. Learning Physical Place and Route in EDA flow.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
CSE A	https://classroom.google.com/w/NDA1Mzg2MTUzMDU5/tc/NDY0MTg5MDI4NDM1
CSE B	https://classroom.google.com/u/0/w/NDAxNDk0MTk5MDUy/tc/NDY0MjY5MDMyMzE0
CSE C	https://classroom.google.com/u/0/w/NDA1MjU0MTk0MDAw/tc/NDY0MjY5Mzc1NjM1
Backlog	https://classroom.google.com/c/NDY0MTkwMTQ2NDQ4?cjc=wc5ve5x