B.TECH/CSE/5TH SEM/CSEN 3104(BACKLOG)/2021

COMPUTER ARCHITECTURE
(CSEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Systolic Array can be thought of as an example of which of the following architecture?
(a) SISD (b) SIMD (c) MISD (d) MIMD

(ii) The number of cycles required to complete n tasks with k stage pipeline is
(a) k+n-1 (b) k (c) nk+1 (d) none of these.

(iii) Which of the following types of instructions are useful in handling sparse matrices in vector processing applications?
(a) Vector – Scalar instruction (b) Masking instruction
(c) Vector – memory instruction (d) None of these.

(iv) The prefetching is a solution for
(a) Data hazard (b) Structural hazard
(c) Control hazard (d) None of these.

(v) Which of the following is an example of 2-dimensional topologies in static network?
(a) Mesh (b) $3C^3$ Network
(c) Linear Array (d) None of these.

(vi)
(1) Virtual Memory	(i) Conflicts
(2) Cache Memory	(ii) Pages
(3) Cache Coherence	(iii) Blocks
(4) Direct Mapped Cache	(iv) Multiprocessor Caches

Which of the following gives the correct matching?
(a) 1-i, 2-ii, 3-iii, 4-iv (b) 1-ii, 2-iii, 3-iv, 4-i
(c) 1-ii, 2-iii, 3-i, 4-iv (d) None of the above.

(vii) A 4-ary 3-cube hypercube architecture has
(a) 3 dimension with 4 nodes along each dimension

(b) 4 dimension with 3 nodes along each dimension
(c) both (a) and (b)
(d) none of these.

(viii) The performance of a pipelined processor suffers if
(a) the pipeline stages have different delays
(b) consecutive instructions are dependent on each other
(c) the pipeline stages share hardware resources
(d) all of these.

(ix) Which of the following is not synonymous to NORMA (No Remote Memory Access) machines?
(a) NUMA (b) Distributed memory multicomputer
(c) Message passing network (d) None of the above.

(x) Stride in vector processor is used to
(a) differentiate different data types (b) registers
(c) differentiate different data (d) None of the above.

Group – B

2. Consider the following reservation table. Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline? Find out simple cycle, greedy cycle and MAL. What are the bounds on MAL?
[(CO2)(CO3)(Remember/IOCQ)]

	1	2	3	4
S1	X			X
S2		X		
S3			X	

(2 + 4 + 4 + 2) = 12

3. (a) Compare Superscalar and Superpipelined architecture. [(CO2)(Understand/LOCQ)]
(b) Explain vector stride and strip mining using examples? [(CO2)(Remember/LOCQ)]
(c) What is instruction level parallelism? [(CO2)(Remember/LOCQ)]
(d) "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement. [(CO1)(Analyze/HOCQ)]

4 + 3 + 2 + 3 = 12

Group – C

4. (a) Draw the diagram of a 8 × 8 Omega Network built with 2 × 2 switching elements. [(CO2)(Remember/LOCQ)]

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously. Does blocking exist in this case? [(CO1)(Analyze/HOCQ)]

6 + (3 + 3) = 12

5. (a) Explain Multistage implementation of a Cube Network with a suitable diagram. [(CO2)(Remember/IOCQ)]

(b) Implement data routing logic of SIMD architecture to compute. [(CO1)(Analyze/HOCQ)]

$$s(k) = \sum_{i=0}^{k} Ai \text{ for } k = 0, 1, 2 \ldots N-1.$$

(c) Why do we need masking mechanism in SIMD array processors? [(CO2)(Remember/LOCQ)]

4 + 5 + 3 = 12

Group – D

6. (a) With simple diagram explain data flow architecture. Compare with Control Flow architecture. [(CO2)(Remember/LOCQ)]

(b) Draw data flow graph for the following set of instructions: [(CO2)(Understand/IOCQ)]

X = A+B
Y=X/B
Z=A∗X
M=Z−Y
N=Z∗X
P=M/N

(c) Explain why Memory-to-Memory architecture is not possible in a Array or Vector Processor Architecture. [(CO1)(Analyze/HOCQ)]

5 + 4 + 3 = 12

7. (a) Develop $3^2 \times 4^2$ delta network. [(CO1)(Analyze/HOCQ)]

(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts: [(CO3)(Analyze/IOCQ)]

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program

(c) What is the significance of interconnection network in multiprocessor architecture? [(CO3)(Understand/IOCQ)]

4 + 5 + 3 = 12

Group – E

8. (a) What is meant by the cache miss penalty? Briefly discuss "early restart" technique to reduce miss penalty. [(CO2)(Understand/LOCQ)]
   (b) Briefly describe cache coherence problem with an example. Suggest one software protocol for this. [(CO2)(Remember/IOCQ)]
   (c) Compare between UMA & NUMA architectures. [(CO2)(Remember/IOCQ)]

(2 + 3)+ (3 + 2) + 2 = 12

9. (a) State for each case mentioned below, which of the following design options are chosen for a RISC based architecture and why? [(CO1)(Analyze/HOCQ)]
   (i) Fixed vs. variable length instruction format
   (ii) Simple vs. complex addressing mode
   (iii) Load-store architecture.
   (b) Explain the fundamental difference in interprocessor communication mechanism between a multiprocessor and a multicomputer system. [(CO2)(Remember/IOCQ)]
   (c) Point out the essential differences between Control Flow and Data Flow machines. [(CO2)(Remember/IOCQ)]

6 + 3 + 3 = 12

Course Outcome (CO):

CO1: Analyze the concept of pipelining, segment registers and pin diagram of CPU.
CO2: Understand and analyze various issues related to memory hierarchy.
CO3: Examine various inter connection structures of multi processor.
CO4. Design architecture with all the required properties to solve state-of-the-art Problems.

LOCQ: 29.17% **IOCQ:** 42.7% **HOCQ:** 28.13%

Department & Section	Submission Link
CSE BACKLOG	https://classroom.google.com/u/1/w/MjgyNTI3NDEyMjc2/tc/MjgyNTI3NDM2MzYx