

**COMPUTER ORGANIZATION
(ECEN 4242)**

Time Allotted : 3 hrs

Full Marks : 70

Figures out of the right margin indicate full marks.

*Candidates are required to answer Group A and
any 5 (five) from Group B to E, taking at least one from each group.*

Candidates are required to give answer in their own words as far as practicable.

**Group – A
(Multiple Choice Type Questions)**

1. Choose the correct alternative for the following: **10 × 1 = 10**
- (i) Which one of the following types of semiconductor memory is used as the main memory in a computer?
(a) SRAM (b) DRAM (c) PROM (d) Flash.
 - (ii) The use of which one of the following in a computer is justified by the principle of locality?
(a) DMA (b) Virtual memory
(c) Software interrupt (d) Cache memory.
 - (iii) Which one the following best describes the organization of a symmetric multiple processor (SMP)?
(a) Single instruction, single data stream
(b) Single instruction, multiple data stream
(c) Multiple instruction, single data stream
(d) Multiple instruction, multiple data stream.
 - (iv) For transferring data from key board to the attached computer, which one of the following would be the preferred mode of transfer?
(a) Direct memory access (DMA) (b) Programmed I/O
(c) Hardware interrupt-driven I/O (d) Software interrupt-driven I/O
 - (v) Von Neumann computers belong to which one of the following classes of computers?
(a) SIMD (b) MIMD (c) MISD (d) SISD.
 - (vi) Instruction pipelining improves CPU performance due to which one of the following reasons?
(a) Reduced memory access time
(b) Use of larger cache
(c) Efficient utilization of the processor hardware
(d) Use of additional functional units.

- (vii) Which one of the following is a major benefit of the Harvard architecture over the Von-Neumann architecture?
- (a) Programs written using single-word instructions execute more quickly than multiword instructions
 - (b) Code and data share memory and increase program execution efficiency
 - (c) Interrupt latency time is very predictable because instructions execute in a single cycle
 - (d) Code and data can be loaded into the CPU simultaneously on separate buses.
- (viii) A processor performing fetch or decoding of different instruction during the execution of another instruction is called?
- (a) Pipe-lining
 - (b) Super-scaling
 - (c) Parallel Computation
 - (d) None of the mentioned.
- (ix) An instruction cycle refers to which one of the following?
- (a) Fetching an instruction
 - (b) Clock cycle time
 - (c) Fetching, decoding, and executing an instruction
 - (d) Executing an instruction.
- (x) Which one of the following types of Interrupts can be caused by an executing program?
- (a) Internal
 - (b) External
 - (c) Hardware
 - (d) Software.

Group – B

2. (a) Discuss in detail about the hardwired control unit with block diagram.
(b) Explain micro program sequencer with proper example?
8 + 4 = 12
3. (a) Describe the major categories of pipeline hazards?
(b) Define parallel processing and explain the Flynn's classification of computer with suitable diagram.
5 + 7 = 12

Group – C

4. (a) How does the size of a cache block affect the hit ratio?
(b) What are the characteristics of SMP and also mention the advantages of SMP organization over a uniprocessor organization?
(c) What do you mean by implicit and explicit multithreading?
2 + (2 + 4) + 4 = 12
5. (a) Define clusters and also discuss the design requirements of clusters?

- (b) Explain branch prediction with the help of proper block diagram?

(2 + 4) + 6 = 12

Group – D

6. (a) Discuss the approaches that are possible to solve the dynamic memory disambiguation problem?
- (b) Explain in detail about the hardware performance issue?
- (c) Write the difference between RISC and CISC processors?

3 + 6 + 3 = 12

7. (a) Elaborate in details about crossbar switch showing the block diagram of functional design of a crossbar switch connected to one memory module?
- (b) Define multicore computer organization and also explain any one example of a heterogeneous multicore chip?

5 + (2 + 5) = 12

Group – E

8. (a) Discuss in details about Berkeley RISC I and also mention its basic addressing modes?
- (b) Describe the data flow diagram of a Two-Stage RISC Pipelined Computer.

8 + 4 = 12

9. Write short notes on any 3 of the following (4 marks each):-

(3 × 4) = 12

- (i) Design of control unit.
- (ii) Memory interleaving.
- (iii) Non-uniform memory access.
- (iv) Symmetric multiprocessors.
- (v) 3-segment instruction pipeline.
- (vi) One-stage of arithmetic logic shift unit.

Department & Section	Submission Link
ECE	https://classroom.google.com/w/MjgwMjY0ODY2NDIy/tc/MzYwMTQyMDA4MjYz