B.TECH/ECE/6TH SEM/ECEN 3233 (BACKLOG)/2021

REAL TIME EMBEDDED SYSTEMS
(ECEN 3233)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For an embedded system, the controller should preferably support:
(a) Two modes; (b) Four modes;
(c)Three modes; (d) Five modes

(ii) The first and last bit of a one-byte UART transmission are ____ and ___ Bits.
(a) Begin, End (b) Start, Stop
(c) Rise, Tail (d) First, Sync.

(iii) The real time signals are:
(a) Analog (b) digital
(c) Hybrid (d) Difficult to predict.

(iv) Watch dog timer is preset with a _____ interval, such that an event must occur during that interval. On failure to get that event in the watched time interval, the device generates the timeout signal.
(a) time (b) data (c) line (d) user.

(v) FLASH is a type of:
(a) ROM (b) RAM (c) OTP ROM (d) EEPROM.

(vi) G sensor is used to sense.
(a) time (b) light (c) sound (d) speed/position.

(vii) In an embedded system, the main challenges are:
(a) Power consumption (b) size (c) cost (d) all of these.

(viii) Daisy chain provides a hardware poll, where I/O devices are connected in order of _____, usually going from highest to lowest.
(a) numbers (b) alphabets (c) practicality (d) priority.

(ix) ARM processors are equipped for:
(a) 16 bit address bus (b) 32 bit data bus
(c) 32 bit address bus (d) 64 bit data bus.

(x) Property which is not included for RTOS is
(a) Deterministic (b) Time Sensitive
(c) Low interrupt latency (d) Can use Virtual Memory.

Group – B

2. (a) How will you differentiate between a general purpose computer and an embedded system? Give the salient features of an ideal embedded system.
What is meant by "bouncing" of an electro mechanical switch? How can it be eliminated using software?

(b) Design a 3 × 8 decoder. Start from the truth table and use K-maps to minimize logic. Develop the final circuit.

(4 + 3) + 5 = 12

3. (a) What is the difference between soft real time system and hard real time system? Explain with examples.
What are the different types of crystal oscillators used for stability? Which is the best and why?

(b) What are the types of architectures used for microprocessors? Explain the differences with the help of block diagrams for both.
Also explain which type is better for DSP and why?

(3 + 3) + 6 = 12

Group – C

4. (a) Indicate whether the 5 following constitute a 'Control', 'Status', or 'Data Transfer' commands.
(i) Skip next instruction if flag is set
(ii) Find a given File on the hard disk
(iii) Check if I/O device is ready
(iv) Move printer head to top of next page
(v) Read interface status register.

(b) Six interface units of the type shown in above Fig. 1 are connected to a CPU that uses an IO address of 8 bits. Each of the 6 chip select (CS) input is connected to a different address line. Thus the high order address line is connected to the CS input of the first interface unit, and the sixth address line is connected to the CS input of the sixth interface unit. The two lower address lines are connected to the RS1 and RS0 of all six interface units. Determine the 8 bit address of each register in each interface.

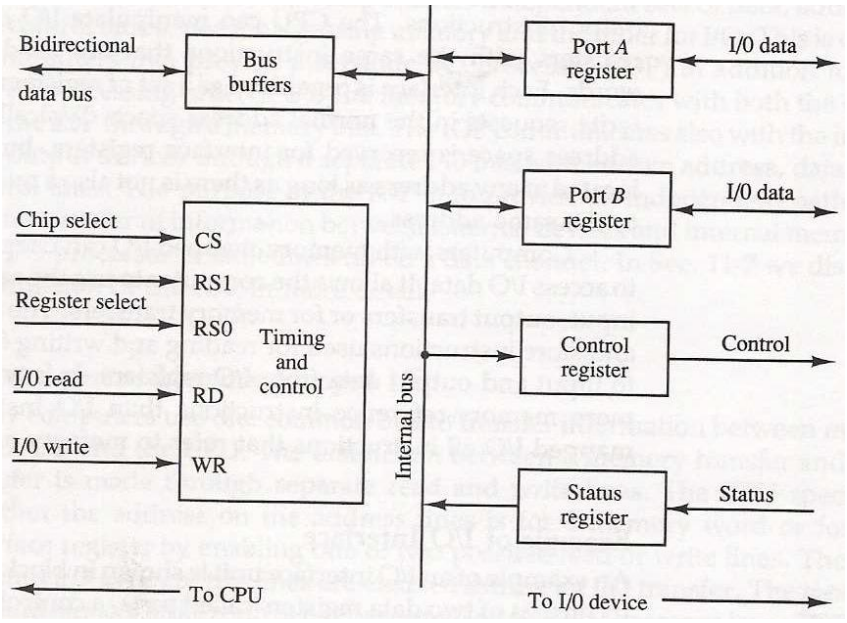

Fig. 1

5 + 7 = 12

5. (a) It is necessary to transfer 256 words from an external hard disk to a memory starting from address 1230. The transfer is by DMA.
   (i) Give the initial values that the CPU must transfer to the DMA controller
   (ii) Give the step by step account of the actions taken during the input of the 1st 2 words.

   (b) A DMA controller transfers 16 bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at 2400 bauds. The CPU is fetching and executing instructions at an average rate of 1 million instructions per sec. By how much will the CPU be slowed down because of the DMA transfer.

(3 + 4) + 5 = 12

Group – D

6. (a) Draw the external block diagram and the internal view of an 8 × 4 ROM chip. What is the difference between OTP and mask-programmed ROM?

   (b) What is 'composing memory'? When is it required? Show how a memory block of size (2^{m+1} x n) can be designed using 2^m x n ROM.

(4 + 2) + (2 + 4) = 12

7. (a) Which types of systems are defined as Multi-rate Systems? Explain with a real time example.

   (b) What is the difference between little-endian and Big-endian mode. Show how the two modes are configured in an ARM processor. What information do the 4 top bits of the CPSR register hold?

(2 + 4) + (1 + 2 + 3) = 12

Group – E

8. (a) Define RTOS characteristics. What are the main difference between GPOS and RTOS?

   (b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is
   (i) immediate
   (ii) direct
   (iii) relative,
   (iv) register in direct
   (v) indexed with R1 as index register.

6 + 6 = 12

9. (a) Define and differentiate between Process, and Threads for an OS.

   (b) Design an adder for two decimal digits represented in excess 3 code. Show that the correction after adding two digits with a 4-bit binary adder is as follows:
   (i) The output carry is equal to the uncorrected carry
   (ii) If output carry = 1, add 0011
   (iii) If output carry = 0, add 1101 and ignore the carry from this addition.
   Show that excess -3 adder can be made with seven full adders and two inverters.

4 + 8 = 12

Department & Section	Submission Link
ECE	https://classroom.google.com/w/OTMyMzg2NjE1NzNa/tc/MzY5MTI0ODk2Njgz