M.TECH/VLSI/2ND SEM/VLSI 5202/2021

VLSI DESIGN, TESTING AND VERIFICATION
(VLSI 5202)

Time Allotted : 3 hrs. **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of physical design is
(a) Layout (b) Mask (c) RTL (d) Circuit Design.

(ii) A MOS device can be used as a resistor in
(a) Linear Region (b) Saturation Region
(c) Sub-threshold condition (d) Mask Region.

(iii) Yield Y = 99% and Fault Coverage T = 90%, DPM (Defects Per Million) is
(a) 10000 (b) 1000 (c) 28,000 (d) 50,000.

(iv) Which among the following has the highest gate integration capacity?
(a) FPGA (b) CPLD (c) PLD (d) ASIC.

(v) VHDL is a
(a) Multi-threaded program (b) C like programming language
(c) Single user program (d) Sequential program.

(vi) Minimum Number of Transistors in TG XOR gate is
(a) 2 (b) 4 (c) 6 (d) 10.

(vii) In the VTC curve of an inverter critical voltages are obtained, where the shape of the curve (dV_{out}/dV_{in}) is
(a) +1 (b) -1 (c) 0 (d) 0.25.

(viii) Synthesis translates descriptions from
(a) Physical to Behavioural (b) Structural to Physical
(c) Behavioural to Structural (d) Structural to Behavioural.

(ix) Average wide delay is changing with Technology advancement in following way
(a) Increasing (b) Decreasing
(c) Remaining same (d) Increasing and then decreasing.

(x) The critical path for a design refers to
(a) the path having maximum delay (b) the path with minimum delay
(c) the path with optimum delay (d) the path with no delay.

Group – B

2. (a) Explain briefly with schematic the operation of a CMOS inverter.

(b) Design a one bit Full Adder, showing the transistor level schematic circuit and also the gate level schematic.

6 + 6 = 12

3. (a) Explain write '1' followed by read '1' operation in 1-Transistor DRAM Circuit using circuit diagram and timing waveforms .

(b) Explain sizing criteria of 6 Transistor SRAM cell.

6 + 6 = 12

Group – C

4. (a) Explain Static Timing Analysis.

(b) Explain PVT corner and worst case design criteria.

6 + 6 = 12

5. (a) Briefly explain interconnect capacitance, and resistance estimation and calculation of interconnect delay techniques.

(b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model.

6 + 6 = 12

Group – D

6. (a) In a flip flop based sequential circuit, Cycle Time = 200ps, Setup Time = 25ps, Clock-Skew = 20ps, Combinational Delay = 60ps, Clock to Out Delay of Flop = 40ps. Hold Time = 40ps. What is setup margin and hold margin for the circuit?

(b) What is clock skew and what are the sources of clock skew?

6 + 6 = 12

7. (a) What is best circuit scheme to create 8 to 256 bit decoder, explain with diagram.

(b) For a Memory Block of 256Kb Memory bits and 32 Data bits, Explain how many row address bits and how many column address bits are needed.

6 + 6 = 12

Group – E

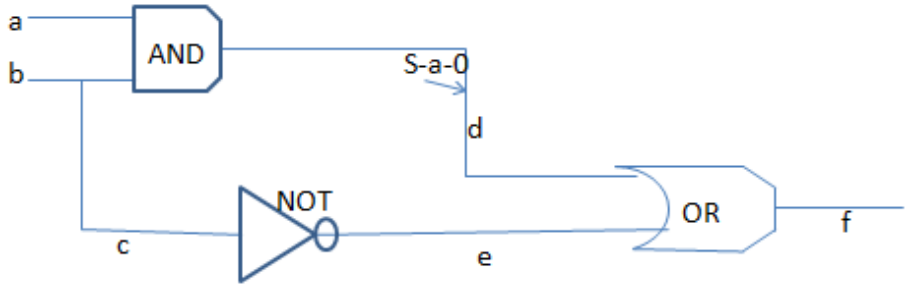
8. (a) What is input test pattern to detect Stuck-at-1 fault at the Output of a 2 input NAND gate?

(b) Explain D-Algorithm using an example.

6 + 6 = 12

9. (a) Explain how Level Sensitive Scan Design Flip Flop (LSSD-SFF) works using Circuit diagram.

(b) Using path sensitization, generate primary input test patterns for S-a-0 fault at line d in the combinational circuit given below.



6 + 6 = 12

Department & Section	Submission Link
VLSI	https://classroom.google.com/c/MzExOTQ2OTQyNjg0/a/MzcxNjUwMTI0MjU3/details