LOW POWER VLSI DESIGN
(VLSI 5232)

Time Allotted : 3 hrs. **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) If Threshold Voltage of transistor is increased 2x, Dynamic power of Digital Gate
(a) Decreases 2x (b) Increases 2x
(c) Remains Same (d) Increases 4x.

(ii) From 65nm Onwards below power is maximum in a chip
(a) Dynamic (b) Leakage
(c) Short Circuit (d) Contention.

(iii) Maximum Leakage Power contribution comes from
(a) Channel Leakage (b) Gate Leakage of ON Transistor
(c) Junction Leakage (d) Gate Leakage of OFF Transistor.

(iv) Memory Cell with Maximum leakage is
(a) SRAM Cell (b) DRAM Cell
(c) ROM Cell (d) Flip Flop Cell.

(v) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L Decreases (b) V_{DD} Decreases
(c) Activity Factor Decreases (d) Chip Frequency Decreases.

(vi) Maximum Leakage reduction in ROM array is possible with
(a) All '0' bits in array (b) All '1' bits in array
(c) 50% '0' bits in array (d) 75% '0' bits in array.

(vii) If P_A is Signal Probability of A input of Inverter, The Signal Probability of Inverter Output is
(a) P_A (b) 1- P_A (c) 1 (d) 0.5.

(viii) If Threshold Voltage of transistor is decreased, Channel Leakage of transistor
(a) Increases Exponentially (b) Decreases Linearly
(c) Decreases Exponentially (d) Remains Same.

(ix) If Rise Time of input of a inverter is increased, then Short Circuit Current
(a) Increases linearly (b) Decreases linearly
(c) Remains Same (d) Decreases Exponentially.

(x) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L Decreases (b) V_{DD} Decreases
(c) Activity Factor Decreases (d) Never Possible.

Group – B

2. (a) If P_A and P_B are Signal Probability of A and B input of an NOR gate, calculate Transition Probability of output Y of NOR gate.

(b) What are various techniques of Activity Factor reductions in digital Gate?

6 + 6 = 12

3. (a) Under what input condition Channel Leakage Power through a 3 input NOR Gate is minimum and why ?

(b) Draw Gate Delay vs Threshold voltage curve for various Supply Voltage of a digital Gate and explain.

6 + 6 = 12

Group – C

4. (a) Why High K plus Metal gate Transistor was introduced for nano Transistors?

(b) How FINFET can save more channel and gate leakage with respect to traditional MOS Transistor for similar performance.

6 + 6 = 12

5. (a) What are various components of Switching Load Capacitance (C_L) in Digital Circuit?

(b) What are various techniques of reducing C_L?

6 + 6 = 12

Group – D

6. (a) Explain how Dual Threshold Voltage devices (High and Nominal Threshold Voltage) can reduce leakage power significantly without compromising chip frequency.

(b) For 3 input NAND gate, mention leaking transistors (channel leakage) for all possible combination of inputs including stacking effect

6 + 6 = 12

7. (a) For 3 input NAND gate, mention leaking transistors (channel leakage) for all possible combination of inputs.

(b) Explain how both channel and gate leakage can be reduced in FINFET Transistor without compromising delay performance with respect to traditional Transistor?

6 + 6 = 12

Group – E

8. (a) Draw Circuit Diagram of 6 Transistor SRAM cell with appropriate interface signals and show sources of various leakage power in SRAM cell?

(b) Why pseudo NMOS logic family is not power friendly?

6 + 6 = 12

9. (a) Why Dynamic Power in memory array is not as critical as data-path circuit ?

(b) How Feed forward inverter in Keeper Circuit can save power of a dynamic logic gate?

6 + 6 = 12

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/MzEyODkyNTYzNTk1/tc/Mzc0MjY2NDE2MDM1