ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 2 hrs. **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The maximum analog output voltage of a DAC
(a) does not equal V_{REF} (b) equals V_{REF}
(c) equals V_{DD} (d) equals ($V_{REF} - V_{th}$).

(ii) If the line width of a spiral is doubled to reduce its resistance with D_{out} , S and N remaining constant, the inductance
(a) Reduces with decrease in diameter of the inner turns
(b) Reduces with reduction in mutual coupling
(c) Both (a) and (b)
(d) Increases with increase in mutual coupling.

(iii) A good current mirror should have
(a) Non-identical drain-source voltages and high output resistance
(b) Identical drain-source voltages and high output resistance
(c) Non-identical drain-source voltages and low output resistance
(d) Identical drain-source voltages and low output resistance.

(iv) The gate-to-channel capacitance of the MOSFET is given as,
(a) $C_{GC} = W_{eff}(L - LD)C_{OX}$ (b) $C_{GC} = W_{eff}(L - 2LD)C_{OX}$
(c) $C_{GC} = W_{eff}(L+LD)C_{OX}$ (d) $C_{GC} = W_{eff}LC_{OX}$
Where, LD stands for lateral diffusion.

(v) The substrate of NMOS transistor is connected to
(a) ground (b) most negative supply in the system
(c) threshold voltage (d) most positive supply in the system

(vi) An ideal differential amplifier should have common-mode voltage gain,
(a) $A_{VC} = 0$ (b) $A_{VC} = 1$ (c) $A_{VC} = \infty$ (d) $0<A_{VC}<1$

(vii) The primary disadvantages of the switched capacitor circuits are
   (a) necessity of the bandwidth of the signal being less than the clock frequency
   (b) necessity of the bandwidth of the signal being greater than the clock frequency
   (c) requirement of non-overlapping clock
   (d) both (a) & (c).

(viii) SFDR is the specification for
   (a) ADC (b) DAC
   (c) Both ADC & DAC (d) All RFIC

(ix) The dynamic range of the DAC can be expressed as,
   (a) 6.02dB (b) – 6.02dB (c) 6.02N dB (d) – 6.02NdB.

(x) The performance of the current sink / source circuit can be improved by
   (a) increasing r_{ds} and reducing V_{MIN} (b) increasing r_{ds} and increasing V_{MIN}
   (c) decreasing r_{ds} and increasing V_{MIN} (d) decreasing r_{ds} and decreasing V_{MIN}

Group – B

2. (a) Explain how V_{MIN} can be reduced in cascode current sink circuit.

   (b) For the circuit in Fig.1, analyze qualitatively what will happen if we inject a current at the location seen in the figure of -1μA ≤ I ≤ 1μA. All MOSFETS are having 10/1 aspect ratios.

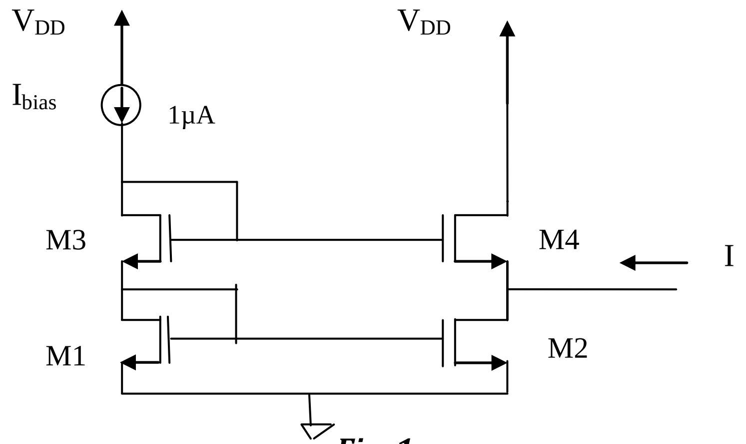

Fig. 1

   (c) Calculate the small-signal voltage gain of the push-pull amplifier.

5 + 4 + 3 = 12

3. (a) Explain the large-signal model for the MOS transistor.

   (b) Explain the dependence of gate-to-source, gate-to-drain and gate-to-bulk capacitance on the gate-to-source voltage for zero body-to-source voltage and constant drain-to-source voltage.

6 + 6 = 12

Group – C

4. (a) Briefly discuss the basic structure of the integrated inductors and how is the inductance related to its dimensions.

(b) If a long wire connecting two circuit blocks carries a high frequency signal, for the wire the current "Return Path" is poorly-defined – explain this attribute and consequences. How are these issues alleviated with integrated T-lines?

(c) Compare the Q of *T*-line inductors with that of spiral inductors.

4 + (3 + 3) + 2 = 12

5. (a) Explain the phenomenon of harmonic distortion in a memory less system.

(b) Briefly discuss Gain Compression in RF Circuits and Systems. Calculate the input 1dB Compression point and also interpret graphically.

(c) For Square Law MOS transistors operating in saturation, the V_{out} vs. V_{in} characteristics can be expressed as

$$V_{out} = -\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{in}R_D\sqrt{\frac{4I_{ss}}{\mu_n C_{ox}\frac{W}{L}} - V_{in}^2}$$

If the differential input is small, approximate the characteristic by a polynomial.

3 + (3 + 3) + 3 = 12

Group – D

6. (a) Explain the data conversion mechanism in an *N-bit* pipeline algorithmic analog-to-digital converter.

(b) If the sampled analog input to a *4-bit* pipeline algorithm *ADC* is 2 volts and $V_{REF} = 5V$, then evaluate the digital output word and the analog equivalent voltage. Show that the ADC will have an error in the fifth bit if the gain of the first stage is 1.875 when $V_{IN} = V_{REF}$.

5 + (5 + 2) = 12

7. (a) Explain the operation of a charge-scaling DAC.

(b) Design a 3-bit charge scaling DAC and find the value of the output voltage for $D_2D_1D_0$ = 1 0 1. Assume that V_{REF} = 5V and C = 0.5pF

6 + 6 = 12

Group – E

8. (a) Why switched-capacitor circuits are preferred for implementing analog signal processing circuits? Draw the configuration of a series-parallel switched capacitor circuit and emulate its equivalent resistance.

(b) For this configuration, find out the capacitor *C* (considering $C_1 = C_2 = C$) that can emulate a *1MΩ* resistor if the clock frequency is *250KHz*.

(2 + 8) + 2 = 12

9. (a) Explain why a single common – source stage does not oscillate if it is placed in a unity gain loop.

(b) Determine the maximum voltage swings and the minimum supply voltage of a ring oscillator incorporating differential pairs with resistive loads if no transistor must enter the triode region. Assume each stage experiences complete switching.

4 + 8 = 12

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/MzExOTI1MzE3ODYw/tc/Mzc0Mjg3OTY5Mzk0