ADVANCED VLSI PROCESSOR
(VLSI 5241)

Time Allotted : 3 hrs. **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For a RISC type machine the Instruction Set Architecture is of type
(a) L/S (b) R/M (c) R+M (d) L/M.

(ii) The _____ architecture uses physically same storage and signal pathways for their instruction and _____.
(a) Harvard, data (b) Von-Neumann, address
(c) Harvard, address (d) Von-Neumann, data.

(iii) Single Pipeline Processors are categorized under
(a) SISD (b) SIMD (c) MISD (d) MIMD.

(iv) TMS320C5X DSPs are said to have advanced _____ architecture because they have _____ memory bus structures for program and data.
(a) Von Neumann, Same (b) Harvard, Alternate
(c) Von Neumann, Separate (d) Harvard, Separate.

(v) The CMAR (Control memory address register) is used when the CU (Control Unit) design type is
(a) Hard-wired (b) Firm-wired
(c) Micro-Programmed (d) Soft-wired.

(vi) ALU is an integral part of the
(a) CU (b) CPU (c) Memory unit (d) I/O unit.

(vii) The three pipeline data hazards are
(a) RAW, WAR, & WAW (b) Store, Memory, Execute
(c) Control, Resource, Data (d) CPU, ALU, GPU.

(viii) Status Registers ST0 and ST1 are of size.
(a) 8 bits each (b) 16 bits each
(c) 8 bits and 16 bits (d) 16 bits and 8 bits.

(ix) Thumb instruction set belongs to which architecture family.
(a) Intel Polaris (b) DSP chip TMS320C5X
(c) ARM (d) DSP5600X from MOTOROLA.

(x) The CMP (Chip Multiprocessor) is made by filling up a processor die with _____, relatively _____ processor cores instead of just one huge core.
(a) simpler, computer (b) multiple, useful
(c) multiple, simpler (d) wafer, fast.

Group – B

2. (a) Sketch the instruction format of a two address instruction that uses immediate, register direct, and indexed addressing mode, if size of the available memory is 1 MB and size of the instruction word is limited to 16 bits with a 3 bit opcode field.

(b) Consider the following register transfer statements for two 4 bit registers R1 and R2 and a 4 bit adder.
xT: R1 ← R1 + R2
x'T: R1 ← R2.
R1 depends on variables T and x. Draw a diagram showing the hardware implementation of the two statements. In the diagram show how the control variables x and T are used to load register R1.

6 + 6 = 12

3. (a) Indicate whether the following constitute a 'Control', 'Status', or 'Data Transfer' commands.
(i) Skip next instruction if flag is set
(ii) Find a given File on the hard disk
(iii) Check if I/O device is ready
(iv) Move printer head to top of next page
(v) Read interface status register.

(b) A non pipeline adder system takes 400 ns to process a task. The same task is processed in a 4 segment pipeline, where the time delay for four segments of the pipeline are as follows, t1=50ns, t2=30ns, t3=95ns & t4=45ns. The interface registers delay time tr=5ns.
(i) How long would it take to add 100 pairs of number in the pipeline?
(ii) Determine the speedup ratio of the pipeline for hundred tasks.
(iii) What is the maximum speedup that can be achieved?

6 + 6 = 12

Group – C

4. (a) Identify the RAW, WAR, and WAW dependencies in the following code segment
I1: R1 = 100;
I2: R1 = R2 + R4;
I3: R2 = R4 – 25;
I4: R4 = R1 + R3

I5: R1 = R1 + 30

(b) What is VLIW? Explain with diagram how higher throughput is obtained using VLIW architecture.

6 + (1 + 5) = 12

5. (a) Explain why the MAC operation is implemented in hardware in programmable DSPs.

(b) List the status register bits of TMS320C5X and briefly explain their functions?

(c) Let the initial content of AR0 register be 2345h and initial content of data memory location 1500h be 6789h. What will be the contents of register AR0 and memory location 1500h after execution of the instruction LMAR AR0, #1500h?

4 + 4 + 4 = 12

Group – D

6. (a) What standard hardware platforms are used as a hardware accelerator? What are the different types of parallelism used in an accelerator?

(b) Describe the register organization in ARM7

(3 + 4) + 5 = 12

7. (a) For ARM Cortex A7 describe the status flags and the program status registers SPSR and CPSR. with its bit structure.

(b) Let initial data content of register r1 be 1000h and memory content of location 1000h, 1004h, and 1008h be 20, 50, and 2 respectively. What will be content of those memory after execution of the following program

```
LDMIA  r1, (r6, r3, r2)
ADD    r5, r6, r3, LSL r2
STMIA  r1, (r5, r2, r6).
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6 + 6 = 12

Group – E

8. (a) State Moore's Law? What is Denard's scaling?

(b) Using Denard's scaling for power, explain the concept of 'Dark Silicon'.

(3 + 4) + 5 = 12

9. (a) What is meant by a pipelined architecture? How does it improve the speed of program execution of a processor?

(b) Describe the pipeline hazards.

(3 + 3) + 6 = 12

Department & Section	Submission Link
VLSI	https://classroom.google.com/w/MzEyOTIwNzk1Njkz/tc/MzcxNjU5NzMyNzMw