DIGITAL VLSI DESIGN
(ECEN 3201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 16 Months (b) 18 Months
(c) 24 Months (d) 30 Months.

(ii) Latest Integration Technology is
(a) LSI (b) VLSI (c) ULSI (d) GSI.

(iii) Value of "Lambda" in 180nm Process Node is
(a) 130nm (b) 65nm (c) 90nm (d) 100nm.

(iv) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(v) Minimum Number of Transistors in CMOS logic Y = AB + CD is
(a) 10 (b) 12 (c) 14 (d) 8.

(vi) LUT belongs to below types of Circuits
(a) Gate Array (b) CPLD (c) PLA (d) FPGA.

(vii) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis.

(viii) Most Noise Immune Logic Family is
(a) NMOS (b) Pseudo NMOS
(c) Dynamic (d) CMOS.

(ix) Most Manual Effort is needed in below VLSI Methodology
(a) FPGA (b) Gate Array
(c) Std Cell Based Semi Custom (d) Full Custom.

(x) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.7 (b) 0.5 (c) 0.45 (d) 0.65.

Group – B

2. (a) What are differences between Full Custom Design and Std Cell based Semi Custom Design ?

(b) Draw Circuit Diagram of 4 input NOR gate using CMOS Logic.

(c) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

4 + 4 + 4 = 12

3. (a) Draw VTC Curve for CMOS Inverter and show various Region

(b) Draw Domino Implementation of 8 input OR gate

(c) Implement f = A.B Boolean logic using Transmission Gate.

3 + 4 + 5 = 12

Group – C

4. (a) Draw Circuit Diagram of a Level-1 D-Latch using CMOS Transmission Gate (TG).

(b) Draw Circuit Diagram of a Positive Edge Triggered D-Flip Flop using D-Latch.

(c) Explain Euler Path solution of a CMOS gate which represents function f = (AB+C+D) ! (! Means Bar) and draw Stick Diagram of the same CMOS gate based on Euler Path Solution.

3 + 3 + (3 + 3) = 12

5. (a) Draw Layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(b) What is the difference between “Micron based Design Rule” and “Lambda Based Design Rule”?

(c) Draw schematic and Stick Diagram of 3 input NAND gate.

4 + 3 + 5 = 12

Group – D

6. (a) Write Verilog Description of a Level-1 D-Flipflop.

(b) Write Verilog Description of a 3 to 8 Decoder.

(c) Write Verilog Description of a 2:1 MUX.

4 + 4 + 4 = 12

7. Write short notes on below topic
(i) FPGA

(ii) Floorplan
(iii) Routing.

4 + 4 + 4 = 12

Group – E

8. (a) What is input test pattern to detect Stuck-at-1 fault at the Output of a 2 input NAND gate ?

(b) Explain D-Algorithm using an example.

6 + 6 = 12

9. (a) Draw Circuit diagram of Scan Flip Flop and explain how it works.

(b) Draw block diagram of Scan Design/Structure and explain its operation.

6 + 6 = 12

Department & Section	Submission Link
ECE	https://classroom.google.com/u/0/w/MzY0NjE3MDkyMjYy/tc/MzY0NjE3MDk4NjA0