DIGITAL SYSTEMS DESIGN
(ECEN 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Simplified form of Boolean expression $(A + \bar{B} + \bar{A}B)C$ is
(a) 1 (b) 0 (c) C (d) $\bar{C}$.

(ii) Which of the following is a self-complementing code?
(a) XS-3 code (b) Gray code
(c) Hamming code (d) Cyclic code.

(iii) The simplified form of the Boolean expression (X + Y + XY)(X + Z) is
(a) X + Y + Z (b) XY + YZ (c) X + YZ (d) XZ + Y.

(iv) The code used for labelling the cells of a K-Map is
(a) 8-4-2-1 binary (b) hexadecimal
(c) gray (d) octal.

(v) $(11011)_2$ in BCD code is
(a) 00011011 (b) 00100111
(c) 11011001 (d) 01101100

(vi) The minimum number of 2-input NAND/NOR gates required to realize a half-adder is
(a) 3 (b) 4 (c) 5 (d) 6.

(vii) A 32:1 MUX can be designed
(a) two 16:1 MUXs and one two input OR gate
(b) two 16:1 MUXs and one two input AND gate
(c) two 16:1 MUXs and two two-input OR gate
(d) two 16:1 MUXs only.

(viii) A flip-flop can store
(a) one bit of data (b) two bits of data
(c) three bits of data (d) any number of bits of data.

(ix) How many stages a 6-bit ripple counter can have?
(a) 6 (b) 12 (c) 32 (d) 64.

(x) How many full adders are required to construct a *m* bit parallel adder?
(a) m/2 (b) m-1 (c) m (d) m+1.

Group – B

2. (a) Simplify the Boolean function by using K-map:
F=∑m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13) and implement the real minimal expression in universal logic.

(b) (i) Add 25+13 in the 8421 BCD code.
(ii) Convert the binary 1001 to the Gray code.

(6 + 2) + (2 + 2) = 12

3. (a) Simplify the Boolean function using tabular method:

$$f(A,B,C,D) = \sum m(1,2,3,5,6,11,12) + \sum d(7,8,10,14)$$

(b) Convert $(78)_{10}$ to gray code.
Convert $(546.77)_8$ to common binary code.

8 + (2 + 2) = 12

Group – C

4. (a) Design a 4-to-16 Decoder using Two 3-to-8 Decoders.

(b) Implement the following function using 4:1 MUX:
F(A, B, C)=∑m(1, 3, 5, 6)

6 + 6 = 12

5. (a) Design a Half-subtractor using only NAND gates.

(b) What are ROM and RAM? What are the basic differences between EPROM and EEROM?

(c) Design a 16:1 multiplexer using 8:1 multiplexers and necessary logic gates.

4 + (2 + 2) + 4 = 12

Group – D

6. (a) Draw the circuit diagram of a positive edge-triggered JK flip-flop and explain its operation with the help of a truth table.

(b) With neat diagrams explain the working of the following types of shift registers.
(i) serial-in parallel-out (ii) parallel-in serial-out.

6 + (3 + 3) = 12

7. (a) What is the difference between asynchronous and synchronous counters?

(b) What are the advantages of a J-K flip-flop over an S-R flip-flop? Realize a D flip flop using T flip flops.

7 + 5 = 12

Group – E

8. (a) Explain the operation of a Dual slope ADC with proper circuit diagram. What is the advantage of R-2R ladder type DAC over counter type DAC?

(b) Define the resolution of DAC. A 6 bit DAC has a step size of 50 mV. Determine the full scale output voltage and resolution.

6 + (2 + 4) = 12

9. Write short notes on any *three* of the followings:
   (i) Look-Ahead-Carry Adder
   (ii) Synchronous Counter
   (iii) Combinational Logic Circuit
   (iv) Latch and Flip-Flop
   (v) Two input TTL NAND gate

(4 + 4 + 4) = 12

Department & Section	Submission Link
ECE Sec A	https://classroom.google.com/c/Mjk5ODAxMzkyNTA3/a/Mzc0MTI1MzQ1OTE5/details
ECE Sec B	https://classroom.google.com/w/MzQyNjA0Mzk4MDIw/tc/Mzc0Mjk3ODE0OTI2
ECE Sec C	https://classroom.google.com/w/MzEyMzk4NTM1NDA0/tc/Mzc0MTM4MTQwMjQ3
BACKLOG	https://classroom.google.com/c/Mzc0Mjk4NzQ3MjE0?cjc=chbaw3g