COMPUTER ORGANIZATION AND ARCHITECTURE
(MCAP 1205)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Cache memory acts between
(a) CPU and RAM (b) RAM and ROM
(c) CPU and Hard Disk (d) None of these

(ii) A Stack-organised computer uses instruction of
(a) Indirect addressing (b) Two-addressing
(c) Zero addressing (d) Index addressing

(iii) The communication between the components in a microcomputer takes place via the address and
(a) I/O bus (b) Data bus
(c) Address bus (d) Control lines

(iv) Data input command is just the opposite of a
(a) Test command (b) Control command
(c) Data output (d) Data channel

(v) Status bit is also called
(a) Binary bit (b) Flag bit
(c) Signed bit (d) Unsigned bit

(vi) In which addressing mode the operand is given explicitly in the instruction
(a) Absolute (b) Immediate
(c) Indirect (d) Direct

(vii) Pipeline implement
(a) fetch instruction (b) decode instruction
(c) fetch operand (d) calculate operand

(viii) When a subroutine is called, the address of the instruction following the CALL instructions is stored in/on the
(a) stack pointer (b) accumulator
(c) program counter (d) stack

(ix) Data hazards occur when .....
(a) Machine size is limited
(b) Pipeline changes the order of read/write access to operands
(c) Some functional unit is not fully pipelined
(d) None of the above

(x) Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
(a) Memory Address Register (b) Memory Data Register
(c) Instruction Register (d) Program Register

Group – B

2. (a) Evaluate the following arithmetic statement using three addresses and two addresses instructions: X=(A+B)*(C+D)

(b) Differentiate between Hardwired control and Microprogrammed Control.

(c) Explain memory-reference instructions format.

4 + 4 + 4 = 12

3. (a) What is a microprogram sequencer? With block diagram, explain the working of microprogram sequencer.

(b) Mention the functions of the following processor registers
(i) IR (ii) MAR (iii) PC.

(c) What is the difference between direct and indirect address instruction?

(1 + 5) + 3 + 3 = 12

Group – C

4. (a) Explain booth's multiplication algorithm with suitable example.

(b) Obtain the differences: (i) 8AA16 - 7CB16 , (ii) 4687 – 7684

6 + 6 = 12

5. (a) What do you mean by fixed point representation? Explain the various integer representations with suitable example.

(b) Explain the overflow condition in arithmetic shift micro operation.

(2 + 5) + 5 = 12

Group – D

6. (a) Write short notes on the following
(i) Direct Memory Access. (ii) Associative Memory.

(b) What is virtual memory? Explain the steps involved in virtual memory address translation.

7 + 5 = 12

7. (a) Compare among different mapping techniques in virtual memory

(b) What do you mean by software of hardware interrupts? How there are used in a microprocessor system?

(2 + 4) + 6 = 12

Group – E

8. (a) What is the difference between serial and parallel transfer? Explain with proper example.

(b) What is Synchronous Bus Transfer? Explain with a timing diagram.

6 + 6 = 12

9. (a) Explain daisy chain priority.

(b) Define strobe control with an example.

(c) What are the different factors that can affect the performance of a pipelined system?

3 + 3 + 6 = 12

Department & Section	Submission Link
MCA	https://classroom.google.com/c/MzcxNzUxOTE1ODkx/a/Mzc0NjI0NDk2MjI2/details