COMPUTER ORGANIZATION AND ARCHITECTURE
(MCAP 1201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Floating point representation is used to store
(a) Boolean values (b) whole numbers
(c) Real integers (d) Integers

(ii) The circuit used to store one bit of data is known as
(a) Register (b) Encoder
(c) Decoder (d) Flip Flop

(iii) Which of the following is lowest in memory hierarchy?
(a) Cache memory (b) Secondary memory
(c) Registers (d) RAM

(iv) Von Neumann architecture is
(a) SISD (b) SIMD
(c) MIMD (d) MISD

(v) The main memory in a Personal Computer (PC) is made of
(a) cache memory. (b) static RAM
(c) Dynamic Ram (d) both (a) and (b)

(vi) The load instruction is mostly used to designate a transfer from memory to a processor register known as
(a) Accumulator (b) Instruction Register
(c) Program counter (d) Memory address Register

(vii) An interface that provides a method for transferring binary information between internal storage and external devices is called
(a) I/O interface (b) Input interface
(c) Output interface (d) I/O bus

(viii) The BSA instruction is_____.
(a) Branch and store accumulator (b) Branch and save return address
(c) Branch and shift address (d) Branch and show accumulator

(ix) Interrupts which are initiated by an instruction are
(a) internal (b) external
(c) hardware (d) software

(x) A pipeline is like _____
(a) an automobile assembly line (b) house pipeline
(c) both (a) and (b) (d) a gas line

Group – B

2. (a) Design a 8 to 1 multiplexer by using the four variable function given by $F(A,B,C,D) = \sum m(0,1,3,6,8,9,14)$.

(b) Simplify the following expression into sum of products using Karnaugh map $F(A,B,C,D) = (1,3,4,5,6,7,9,12,13)$.

6 + 6 = 12

3. (a) What is encoder? Draw the logic circuit of a 3 line to 8 line decoder and explain its working.

(b) Why do 11 come before 10 in the K-map?

(c) Simplify the Boolean expression F = C(B + C)(A + B + C).

5 + 2 + 5 =12

Group – C

4. (a) With relevant diagram explain the working of master-slave SR flip flop.

(b) What is difference between synchronous counter and asynchronous counter?

(c) What is a shift register? Can a shift register be used as a counter? If yes, explain how?

6 + 3 + 3 = 12

5. (a) Evaluate the arithmetic statement X = (A*B)+(C*D) using a general register computer with three address, two address and one address instruction format.

(b) Convert D flip-flop to a JK flip-flop. You can use additional circuiting if required.

6 + 6 = 12

Group – D

6. (a) Evaluate the following arithmetic statement using three addresses and two addresses instructions: X=(A+B)*(C+D).

(b) Differentiate between Hardwired control and Microprogrammed Control.

(c) Explain memory-reference instructions format.

4 + 4 + 4 = 12

7. (a) Compare among different mapping techniques in virtual memory

(b) What do you mean by software of hardware interrupts? How there are used in a microprocessor system?

7 + 5 = 12

Group – E

8. (a) What is asynchronous data transfer? Explain in details? Explain Daisy Chain Priority.

(b) Explain Flynn's classification of computers architecture.

(2 + 2 + 2) + 6 = 12

9. (a) What is the difference between vector and array processing? What is the difference between serial and parallel transfer?

(b) What are the different factors that can affect the performance of a pipelined system?

(3 + 3) + 6 = 12

Department & Section	Submission Link
MCA	https://classroom.google.com/c/MzcxODg2NTI4MDc3/a/Mzc0NjI3OTMyMDcy/details