VLSI DESIGN
(ECEN 4282)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For the successive phenomena of Accumulation, Depletion and Inversion in n-channel Enhancement Type MOSFET, the polarities of the Gate Voltage are ____, _____ and _____ respectively
(a) Positive, Negative, Positive (b) Negative, Positive, Positive
(c) Negative, Negative, Positive (d) Positive, Negative, Negative.

(ii) Cut-Off Mode in n-channel Enhancement Type MOSFET is indicated by
(a) $V_{GSn} = V_{tn}$ (b) $V_{GSn} > V_{tn}$
(c) $V_{GSn} < V_{tn}$ (d) None of the above.

(iii) Linear Mode in p-channel Enhancement Type MOSFET is indicated by
(a) $V_{DSp}>(V_{GSp} - V_{tp})$, $V_{GSp}<V_{tp}$ (b) $V_{DSp} = (V_{GSp} - V_{tp})$, $V_{GSp}>V_{tp}$
(c) All of the above (d) None of the above.

(iv) For the Logic Function, f(A, B, C) = (A.B + C)' implemented by CMOS Logic, the total number of transistors required is
(a) 2 (b) 6 (c) 3 (d) 4.

(v) On increasing the channel length of pMOS transistor in Pull-Up of CMOS Inverter, the VTC shifts to the
(a) Right (b) Left
(c) All of the above (d) None of the above.

(vi) In n Input NAND Gate, all the nMOS transistors in Pull Down are in ____ and all the pMOS transistors in Pull Up are in ____
(a) Series, Parallel (b) Parallel, Parallel
(c) Parallel, Series (d) Series, Series.

(vii) In p-channel Depletion Type MOSFET, the Depletion Gate Voltage is
(a) Zero (b) Positive (c) Negative (d) None of the above

(viii) In n-channel Enhancement Type MOSFET, the Threshold Gate Voltage is
(a) Positive (b) Zero
(c) Negative (d) All of the above.

(ix) If the Aspect Ratio of CMOS Inverter is decreased, then VTC shifts to the
(a) Right (b) Left
(c) All of the above (d) None of the above.

(x) In NAND Gate of 2 Inputs (A and B), the fault of Input, A, being stuck at '1' is detected by the Test Vector
(a) A = 1, B = 1 (b) A = 1, B = 0
(c) A = 0, B = 1 (d) A = 0, B = 0

Group – B

2. (a) Describe the operation of CMOS Inverter (NOT Gate).

(b) Explain why at least 2 Inverters are required to construct a Buffer (Complementary of Inverter) in CMOS Logic.

6 + 6 = 12

3. (a) Construct and explain the operation of CMOS D-Latch.

(b) Implement the following :-
(i) AND Gate by Pass Transistor
(ii) OR Gate by Pass Transistor
(iii) XOR Gate by Transismission Gate.

6 + 6 = 12

Group – C

4. (a) In Full Adder of 3 Inputs, A, B and C_{in} (Input Carry) and 2 Outputs, C_O (Output Carry) and S_O (Output Sum), detect the fault of C_{in} (Input Carry) being stuck at '0' by D-Algorithm.

(b) Explain why Testing is required in VLSI Circuits.

8 + 4 = 12

5. Determine the Test Vectors in order to detect the following faults :- **(6 × 2) = 12**
(i) Input (B) stuck at '1' in NAND Gate of 2 Inputs A and B.
(ii) Input (A) stuck at '0' in XOR Gate of 2 Inputs A and B.
(iii) Input (B) stuck at '1' in NOR Gate of 2 Inputs A and B.
(iv) Input (A) stuck at '0' in XNOR Gate of 2 Inputs A and B.
(v) Input (B) stuck at '1' in XNOR Gate of 2 Inputs A and B.
(vi) Input (A) stuck at '1' in NOR Gate of 2 Inputs A and B.

Group – D

6. (a) Explain what is meant by HDL ?

(b) Explain the difference between Behavioural Verilog Modelling and Data Flow Verilog Modelling.

5 + 7 = 12

7. (a) Explain FSM.

(b) Explain the architecture and functioning of Mealy Machine and Moore Machine.

5 + 7 = 12

Group – E

8. (a) Explain the design and functioning of SRAM and DRAM.

(b) State the types of memory.

8 + 4 = 12

9. (a) Explain the design and functioning of MASK ROM and Flash ROM.

(b) Explain Memory Organization.

8 + 4 = 12

Department & Section	Submission Link
CSE	https://classroom.google.com/w/Mjk5NDAzODA4MjUy/tc/MzU5NTEzMTkxMTEz