COMPUTER ORGANIZATION AND ARCHITECTURE
(CSEN 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Address for the next instruction to be executed is available in the
(a) Program Counter (b) Stack Pointer
(c) Instruction Register (d) Relocation Register.

(ii) Conflict miss can be eliminated, in case of
(a) Direct mapping cache (b) Fully associative cache
(c) Set Associative cache (d) Can never be eliminated.

(iii) Interrupt request is acknowledged by the CPU,
(a) Immediately as soon as the request is generated
(b) After completion of the current machine cycle
(c) After completion of the current instruction cycle
(d) After completion of the currently executing program.

(iv) How many 4 × 3 crossbar switches are required to implement a $4^2 \times 3^2$ Delta Network?
(a) 12 (b) 7 (c)14 (d) 9.

(v) The number of cycles required to complete n tasks with k stage pipeline is
(a) k (b) nk+1 (c) k+n-1 (d) n/k

(vi) Which of the following types of instructions are useful in handling sparse matrices in vector processing applications?
(a) Vector-scalar instruction (b) Vector-memory instruction
(c) Masking instruction (d) Gather-Scatter instruction.

(vii) How many stages of 2 × 2 switches are required to build a 64 × 64 Omega Network?
(a) 3 (b) 4 (c) 6 (d) 64.

(viii) The n numbers of routing functions of an n-dimensional cube network are given by C_0, C_1, C_2, …, C_{n-1}. Then the Exchange Function E(A) is equivalent to
(a) $C_0(A)$ (b) $C_1(A)$ (c) $C_{n-2}(A)$ (d) $C_{n-1}(A)$

(ix) The speedup of a k-stage pipelined processor to complete n tasks, compared to a non-pipelined processor is
(a) n / (k+n -1) (b) n / (k*n -1)
(c) n*k / (k+n-1) (d) n*k / (k*n -1).

(x) Which one of the following statements is true for the direct mapping cache?
(a) FIFO is the best page replacement policy
(b) LRU is the best page replacement policy
(c) Optimal is the best page replacement policy
(d) No page replacement policy is required.

Group – B

2. (a) Evaluate the arithmetic statement X = (A + B) - (C + D) using (i) zero address instructions and (ii) two address instructions.

(b) In a computer, there are 30 processor Registers, 6 addressing modes and 32K X 32 main memory. Each instruction (having size of 32 bits) supports one register operand and one memory address operand. State the instruction format, after finding out the size of each field.

(c) Differentiate between Von Neumann architecture and Harvard architecture. How Von Neumann bottleneck can be minimized?

(2 + 2) + 4 + (2 + 2) = 12

3. (a) What are the advantages of micro-programmed control over hardwired control?

(b) Explain, with an example, Register Indirect Addressing Mode? What is its advantage?

(c) Which Addressing Mode is used for accessing the array elements in sequence? In a relative (PC-relative) addressing, there is a "BR 30" instruction (instruction length = 1 word) at the word address 204F (Hex). What will be the content of the Program Counter after execution of the instruction? (Assume the number 30 is in decimal).

(d) Mention two important points of difference between RISC and CISC.

3 + (3 + 1) + (1 + 2) + 2 = 12

Group – C

4. (a) In a hierarchical memory system, cache access time is 100ns and main memory access time is 1000ns. Hit ratio of cache is 0.9 for read access and 85% of the memory requests are for read. Calculate the average access time of the memory system for both read and write requests. Consider Write Through policy.

(b) From the entry in a segment table, it is understood that segment #0 has base address 215 and length of 500 words, segment #1 has base address 2000 and length of 160 words, segment #2 has base address 1200 and length of 40 words. Find out the physical addresses corresponding to the following logical addresses?
(i) 0, 430 (ii) 1, 234 (iii) 2, 13 (iv) 1, 100

(c) Briefly describe any two techniques to reduce Cache Miss Rate.

4 + 4 + 4 = 12

5. (a) With the help of a block diagram, briefly explain Direct Memory Access.

(b) Briefly explain, with a diagram, Daisy Chaining method for Bus Arbitration.

(c) Describe briefly, the steps involved after an external IO device requests the processor to transfer data by activating the interrupt signal on the CPU.

4 + 4 + 4 = 12

Group – D

6. Consider the Reservation Table given below:

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

(i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector.
(ii) Draw the state diagram for scheduling the pipeline
(iii) List all simple cycles. Especially point out the Greedy Cycles (GC).
(iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL?

(3 + 3 + 3 + 3) = 12

7. (a) Explain, with examples, Gather and Scatter instructions in Vector processing.

(b) Explain vector chaining and vector stride using examples.

(c) In a Vector Processor, the length of the vector registers is 64. Vector addition of two vectors (A and B), each having 140 elements, is required to be performed. How many loops are generated by the Strip Mining Technique and what are the numbers of iterations in each loop?

4 + 4 + 4 = 12

Group – E

8. (a) Consider a 4 × 2 Array Processor with 2 processing elements (PEs) in each of the 4 rows and 4 processing elements (PEs) in each of the 2 columns. Load the

eight numbers 12, 4, 91, 1, 82, 17, 63, 50 in the PEs with snakelike row-major indexing. With the help of diagrams, show the various operations performed in the M(4,2) sorting algorithm to sort the above array.

(b) Illustrate the necessity of data routing in an array processor by showing the execution details to compute:

$$S(k) = \sum_{i=0}^{k} A_i \qquad \text{for } k = 0, 1, \ldots\ldots, (n-1)$$

7 + 5 = 12

9. (a) Draw the diagram of a $3^2 \times 4^2$ Delta network.

(b) Draw the diagram of a multi-stage 8 × 8 Omega network. On the diagram, show the path (along with switch settings) for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously. Does blocking exist in this case?

4 + (3 + 2 + 2 + 1) = 12

Department & Section	Submission Link
CSE - A	https://classroom.google.com/u/1/w/MzA3NDM4NTY1NDQx/tc/MzcxNjYzMTk5Mjgw
CSE - B	https://classroom.google.com/w/MzEyOTAwMjM0ODAy/tc/Mzc0MzUxOTYyODYy
CSE - C	https://classroom.google.com/c/MzExNjA0OTI4MDc1/a/MzcxNjYzMDU0OTk0/details