# COMPUTER ORGANIZATION AND ARCHITECTURE
# (INFO 2203)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
## (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The pipelining process is also called as _____
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) None of the mentioned

(ii) The periods of time when the unit is idle is called as _____
(a) Stalls (b) Bubbles
(c) Hazards (d) Both Stalls and Bubbles

(iii) _____ have been developed specifically for pipelined systems.
(a) Utility software (b) Speed up utilities
(c) Optimizing compilers (d) None of the mentioned

(iv) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order
(c) Out of order (d) None of the mentioned

(v) The step where in the results stored in the temporary register is transferred into the permanent register is called as _____
(a) Final step (b) Commitment step
(c) Last step (d) Inception step

(vi) Both the CISC and RISC architectures have been developed to reduce the _____
(a) Cost (b) Time delay
(c) Semantic gap (d) All of the mentioned

(vii) The BOOT sector files of the system are stored in _____
(a) RAM (b) Hard disk
(c) Fast solid state chips in the motherboard (d) ROM

(viii) Which of the following technique/s used to effectively utilize main memory?
(a) Dynamic linking (b) Dynamic loading
(c) Both Dynamic linking and loading (d) Address binding

(ix) If a system is 64-bit machine, then the length of each word will be _____
(a) 12 bytes (b) 16 bytes
(c) 4 bytes (d) 8 bytes

(x) During the transfer of data between the processor and memory we use _____
(a) TLB (b) Buffers
(c) Cache (d) none of the above

## Group – B

2. (a) Register R1 and R2 of a computer contain the values 1200 and 4600.What is the effective address of the memory operand in each of the following instructions?
(i) Load 20(R1),R5
(ii) Move #3000,R5
(iii) Store R5,30(R1,R2)
(iv) Add -(R2),R5
(v) Subtract (R1)+,R5

(b) Explain with diagram, a n-bit ripple-carry adder. Explain with diagram, a 4-bit carry-lookahead adder.

**5 + (3 + 4) = 12**

3. (a) Design a 1-bit ALU which will perform following operations
(i) Addition (ii) Subtraction (iii) AND (iv) NOR

(b) Multiply the following pairs of signed 2's-complement numbers using the Booth algorithm. Assume that A is the multiplicand and B is the multiplier. A= 010111 and B=110110.

**(2 × 4) + 4 = 12**

## Group – C

4. (a) Consider the following page references and calculate the hit and miss ratio applying LRU and FIFO algorithm (let cache memory has 4-page frames).
4 2 1 5 6 4 3 2 1 4 2 1

(b) A memory system consists of cache, main and virtual memory. Hit rate in cache is 85% and hit rate in RAM is 87%. Calculate the average memory access time if it takes 4 cycles to access the cache, 60 cycles to fetch memory line and 3000 cycles to access virtual memory.

**6 + 6 = 12**

5. (a) A cache memory has the following specifications:-
It has 128 blocks and organizes in 4-way set associativity. Main memory contains 16384 blocks. Each block contains 128 words of 16 bit. Find the bits required for physical address and tag bit comparator.

(b) A memory system having cache and main memory takes 6 cycles to complete cache hit and 2000 cycles to complete a cache miss. Find the T average if miss rate in the cache is 89 percent.

**6 + 6 = 12**

## Group – D

6. Consider the five-stage pipelined processor specified by the following reservation table.

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| S1 | X | | | | | X |
| S2 | | X | | | X | |
| S3 | | | X | | | |
| S4 | | | | X | | |
| S5 | | X | | | | X |

(i) List the set of forbidden latencies and the collision vector.
(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.
(iii) List all the simple cycles from the state diagram.
(iv) Identify the greedy cycles among the simple cycles.
(v) What is the minimum average latency (MAL) of this pipeline?

**(2 + 4 + 2 + 2 + 2) = 12**

7. (a) This problem compares the performance of superpipelined superscalar processor of degree (m,n) with that of a base scalar processor of degree(1,1). Analyse the following speedup expression for the below mentioned limiting case
$S(m,n) = mn(k+N-1)/mnk+N-m$
where N=number of independent instructions and k= number of pipeline stages
i) Within the range $1 <= m <= 4$ and $1 <= n <= 6$, what is the optimal number of pipeline stages that would maximize the speedup S(m,n)?

(b) Consider the execution of a program of 15000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence are ignored.
(i) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non pipelined processor with an equal amount of flow-through delay.
(ii) What are the efficiency and throughput of this pipelined processor?

(c) State the design parameters for pipeline processors.

**4 + (3 + 3) + 2 = 12**

## Group – E

8. (a) Write down the advantages and disadvantages of distributed shared-memory architecture.

(b) Difference between multiprocessor and multicomputer system. What is the benefit of using multiprocessor?

**6 + (4 + 2) = 12**

9. (a) Write the general characteristics of Uniform Memory Access (UMA) and Non-Uniform Memory Access (NUMA) architecture.

(b) Explain the differences among UMA, NUMA, COMA and NORMA computers.

**6 + 6 = 12**

| Department & Section | Submission Link |
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| IT | https://classroom.google.com/c/Mjk4ODQ0MjIwNjE5/a/Mzc0MTk1NTE2MDI3/details |