B.Tech/BT/CE/CHE/EE/IT/1st Sem/ECEN-1001/2015

2015

BASIC ELECTRONICS ENGINEERING

(ECEN 1001)

Time Alloted : 3 Hours *Full Marks : 70*

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : **[10×1=10]**

i) The width of the depletion layer of a junction
   (a) decreases with light doping.
   (b) increases with heavy doping.
   (c) is independent of applied voltage.
   (d) increases under reverse bias.

ii) Temperature coefficient of Zener breakdown voltage
   (a) is negative (b) is positive
   (c) has no effect (d) is none of these

iii) The ripple factor of power supply is a measure of
   (a) its filter efficiency. (b) diode rating.
   (c) its voltage regulation. (d) purity of power output.

iv) For Self sustained oscillation the condition is
   (a) $A\beta > 1$ (b) $A\beta < 1$
   (c) $A\beta = 1$ (d) both (b) & (c)

v) Which of the following statement is not true in case of FET?
   (a) It has high input impedance
   (b) It is noisier than bipolar transistor
   (c) It has large gain-bandwidth product
   (d) All of above

vi) An ideal Op-Amp has
   (a) infinite A_v. (b) infinite R_i.
   (c) zero output resistance. (d) all of the above.

vii) Which one of the following feedback topologies offers high input impedance?
   (a) Voltage Series. (b) Voltage Shunt.
   (c) Current Series. (d) Current Shunt.

viii) Fermi level of an n-type semiconductor lies
   (a) near the conduction band edge.
   (b) near the valence band edge.
   (c) at the middle of the band gap.
   (d) none of these.

ix) The diode in which impurities are heavily doped is
   (a) Varactor diode. (b) PIN diode.
   (c) Tunnel diode. (d) Zener diode.

x) A transistor in common emitter mode has
   (a) a high input resistance and low output resistance.
   (b) a medium input resistance and high output resistance.
   (c) a very low input resistance and a low output resistance.
   (d) a high input resistance and a high output resistance.

GROUP - B

2. (a) What is meant by tunneling phenomenon?

   (b) Discuss how a depletion layer is formed in a P-N diode and how does it vary with biasing?

   (c) Draw V-I characteristics of P-N junction diode.

   (d) The reverse saturation current at 300K of a P-N junction diode (Ge) is 5 μA. Find the voltage to be applied across the junction to obtain a forward current of 50mA.

2+4+3+3 = 12

3. (a) Compare the operation of a Full wave rectifier and a Bridge rectifier.

   (b) Determine the ripple factor and rectification efficiency of a Full wave rectifier.

   (c) A Full wave rectifier use double diode, the forward resistance of each element being 200 ohm. The rectifier supplies current to load resistance of 1000 ohm. The primary to total secondary turns ratio of the centered tapped transformer is 1 : 3. The transformer primary is fed from a supply of 240 V (rms).

   Find (i) the DC load current (ii) the diode current in each diode (iii) the ripple voltage across the load resistance (iv) the efficiency of rectification.

4+3+5 = 12

GROUP - C

4. (a) Explain the mechanism of current flow in a PNP transistor. Why is the collector current slightly less than emitter current?

   (b) Define α and β. Show that $\beta = \frac{\alpha}{(1-\alpha)}$

   (c) Why Common emitter configuration is mainly used?

   (d) The reverse saturation current in NPN transistor in Common Base configuration is 15.5 μA. For an emitter current of 4 mA, collector current is 2.47 mA. Find the value of current gain and base current.

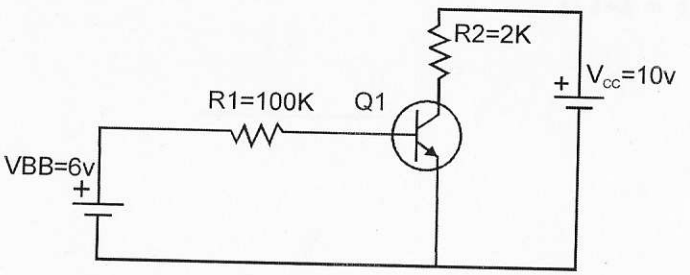
4+2+2+4 = 12

5. (a) What do you understand by transistor biasing? Name the different methods used for transistor biasing.

   (b) What do you mean by thermal runaway?

   (c) Draw the circuit diagram of Self Emitter bias and explain why it has better stability?

   (d) Calculate VCE and Ic in the circuit given below. Assume VBE = 0.7V and β = 50.



2+2+4+4 = 12

Group - D

6. (a) Define the three FET parameters g_m, r_d and μ. Prove that $\mu = g_m.r_d$

   (b) Discuss the similarities and differences between JFET and MOSFET with regard to their construction and applications.

   (c) What do you mean by a pinch-off condition of JFET?

4+5+3 = 12

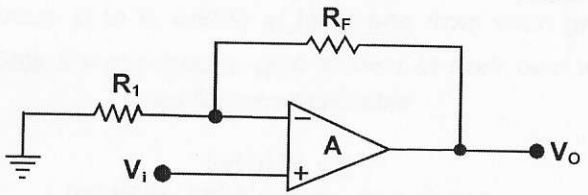
7. (a) Differentiate between enhancement type and depletion type MOSFET. What do you mean by the threshold voltage?

   (b) Draw an n channel enhancement type MOSFET diagram with proper biasing.

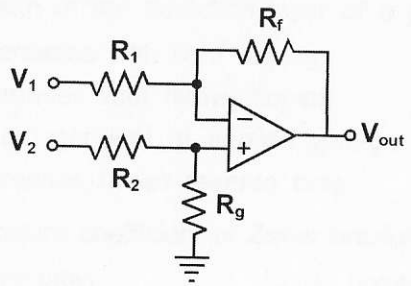
   (c) Explain why the channel is tapered towards drain terminal of an enhancement type MOSFET. **(3+2)+3+4 = 12**

GROUP - E

8. (a) Determine the voltage gain for the circuit shown in fig. below with R_F = 100 KΩ and R_1 = 10 KΩ.



   (b) Determine the output voltage (V out) of the circuit below.

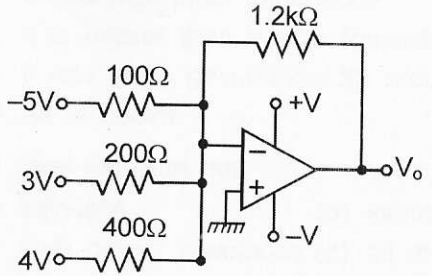


   (c) Show that different feedback topologies with block diagrams for each. **3+3+6 = 12**

9. (a) Discuss the effect of positive feedback amplifier. State and explain the Barkhausen criterion.

   (b) Explain virtual ground concept of an OPAMP. Define the terms CMRR and Slew Rate.

   (c) Find the voltage output of the following circuit.



4+4+4 = 12