DIGITAL ELECTRONICS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The logic function $AB + \overline{A}C + BC$ is equivalent to
(a) A+BC (b) A+ABC
(c) $AB + \overline{A}C$ (d) $\overline{A} + \overline{B}\overline{C}$

(ii) An 8 bit adder circuit requires _____.
(a) 4 full adders and 4 half adders (b) 8 full adders
(c) 7 full adders and one half adder (d) 1 full adder and 7 half adders

(iii) A buffer can be realized by a 2- input X-OR gate when
(a) both inputs are at logic 1 (b) one input is at logic 0
(c) one input is at logic 1 (d) both inputs are at logic 0

(iv) Gray code is advantageous as it requires
(a) moderate switching activity (b) maximum switching activity
(c) minimum switching activity (d) none of the above

(v) 2's complement of 11001011 is _____
(a) 01010111 (b) 11010100
(c) 00110101 (d) 11100010

(vi) The terminal count of a typical modulo-15 binary counter is _____
(a) 1000_2 (b) 1110_2
(c) 1111_2 (d) 1101_2

(vii) The range of decimal numbers for n-bit signed binary representation in 2's complement form is
(a) 1 to $(2^{n-1}-1)$ (b) $+(2^{n-1}-1)$ to $-(2^{n-1})$
(c) $+(2^{n-1}-1)$ to $-(2^{n-1}-1)$ (d) $-(2^{n-1}-1)$ to (-1)

(viii) How many flip-flops are required to make a MOD-15 counter?
(a) 3 (b) 8 (c) 9 (d) 4

(ix) Asynchronously connected three T flip-flops with T = 1 has a 12 KHz clock input. The Q output is

(a) a 6 KHz square wave (b) constantly high
(c) a 3 KHz square wave (d) constantly low

(x) If the number of bits in the sum exceeds the number of bits in each added numbers, it results in _____

(a) Successor (b) Overflow
(c) Underflow (d) Predecessor

Group – B

2. (a) Design and explain the operation of a circuit to perform addition as well as subtraction of 4-bit numbers.

(b) What is the advantage of carry look ahead (CLA) logic to design full adder circuit?

8 + 4 = 12

3. (a) Design a 4-bit binary to gray code converter.

(b) Realize a 16:1 multiplexer by using 4:1 multiplexers.

7 + 5 = 12

Group – C

4. (a) Minimize the logic function
$Y(A,B,C,D,E) = \sum m(0,2,3,5,7,8,10,11,14,15,16,18,24,26,27,29,30,31)$
by using Karnaugh map.

(b) Design a D- flip flop with characteristic table using only NAND gates.

8 + 4 = 12

5. (a) What is the racing problem in J-K flip flop? Explain the remedy of this problem with necessary circuit and wave forms.

(b) What is the difference between flip-flop and latch?

(3 + 6) + 3 = 12

Group – D

6. (a) Design and explain with output waveforms of a frequency divider circuit of which input frequency is 8KHz and output frequency is 500Hz.

(b) Design an asynchronous counter to start the count at $(6)_{10}$ and stop the count at $(13)_{10}$ and start the count again from $(6)_{10}$.

6 + 6 = 12

7. (a) Design a ripple counter to start the count at 2 and stop the count at 12 and start the count again from 2.

   (b) Write short note on Ring counter.

8 + 4 = 12

Group – E

8. (a) Implement the given functions using programmable logic array (PLA) P(a,b,c,d)=∑m(1,2,9,10), Q(a,b,c,d)=∑m(8,10,12,14) and R(a,b,c,d)=∑m(1,3,9,11).

   (b) Write short notes on Flash type ADC and R-2R Ladder type DAC.

6 + (3 + 3) = 12

9. (a) Implement the following logic functions using PROM.
   A = ∑m(0,2,4,6,8), B=∑m(1,3,5,7), C=∑m(0,2,7,11)

   (b) Design and explain the operation of a 2 input NOR and NAND gate using TTL logic.

6 + (3 + 3) = 12

Department & Section	Submission Link
AEIE	https://classroom.google.com/c/MzEyNTA2OTc2MjQx/a/Mzc0NDQwNDU5ODkw/details