DIGITAL LOGIC
(ECEN 2104)

Time Allotted: 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

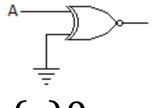
1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) An universal gate is the………………
(a) NAND Gate (b) OR Gate
(c) AND Gate (d) None of the above.

(ii) If the output of a logic gate is 1 when all its inputs are at logic 1, then the gate is either
(a) an OR or an X-OR (b) a NAND or an X-NOR
(c) an AND or a NAND (d)an OR or an X-NOR,

(iii) 2’s complement of a four bit binary number 0101 is ………..
(a)1011 (b)1111 (c)1101 (d)1110.

(iv) For the Gate in the given figure below, the output will be ………..



(a)0 (b)1 (c) A (d) $\bar{A}$.

(v) A 32×10 ROM contains a decoder of size
(a) 5×32 (b) 32×32
(c) 32×10 (d) 10×32.

(vi) How many full-adders are required to construct an m-bit parallel adder?
(a) m/2 (b) m-1 (c) m (d) m+1.

(vii) The characteristic equation of a S-R flip-flop is
(a) $Q_{n+1} = Q_n\overline{R} + S$ (b) $Q_{n+1} = \overline{Q_n}R + S$
(c) $Q_{n+1} = Q_nR + \overline{S}$ (d) $Q_{n+1} = Q_n$.

(viii) How many Flip-Flops are required for a Mod–16 Counter ?
(a) 5 (b) 6 (c) 3 (d) 4.

(ix) Which of the memory is a volatile memory?
(a) ROM (b) RAM (c) PROM (d) EEPROM.

(x) The Digital Logic Family which has the lowest propagation delay time is
(a)ECL (b) TTL (c) CMOS (d) PMOS

Group – B

2. (a) Implement the following Boolean function using 8:1 multiplexer:
$F(A,B,C,D) = A\overline{B} + BD + B\overline{C}\overline{D}$

(b) Find the minimal SOP form for the Boolean expression $f(A,B,C,D)=\sum m(1,3,4,5,9,10,11) + \sum d(6,8)$.

6 + 6 = 12

3. (a) Implement the following Arithmetic Operations by 2's Complement Method :-
(i) 15–12
(ii) -12-15

(b) Perform the BCD addition $(695)_{BCD}+(594)_{BCD}$ mentioning all the steps clearly.

(3 + 3) +6 = 12

Group – C

4. (a) Design a 3 bit even parity generator and the corresponding 4 bit even parity checker circuit.

(b) For a four input logic function, $Y = f(I_3, I_2, I_1, I0)$, the output Y is 0 when the decimal equivalent of the binary values of the input variables $(I_3I_2I_1I_0)$ is a prime number (for example, $I_3=0$, $I_2=1$, $I_1=1$, $I_0=1$, implies $(I_3I_2I_1I_0) = (0111)_2 = (7)_{10} = 7$. As 7 is a prime number then the output is 0) otherwise the output Y is 1. Implement the logic circuit of the given function by a 4:1 multiplexer and external gates.

(3 + 3) + 6 = 12

5. (a) Explain the advantages of a priority encoder over a standard encoder using illustrative examples with 4-line to 2-line standard encoder and a priority encoder.

(b) Implement a 8-to-1 line multiplexer using 4-to-1 line multiplexers.

8 + 4 = 12

Group – D

6. (a) Convert a S-R flip flop to D, J-K and T flip flop.

(b) What is a 'race around' condition in a flip flop? How is it eliminated?

(2 + 2 + 2) + (4+2) = 12

7. (a) Design a 4 bit register using D flip flops.

(b) Design a 4 bit asynchronous up and down counter.

6 + 6 = 12

Group – E

8. (a) Explain the logic operation of the CMOS inverter.

(b) Design a CMOS NAND gate and a CMOS OR gate.

(6) + (3+3) = 12

9. (a) Construct a two input NAND gate using CMOS logic and clearly explain its operation.

(b) Write two advantages of using CMOS logic.

(c) Realize the following logic expression using CMOS logic
F= $\overline{AB+CD}$

5 + 2 + 5 = 12

Department & Section	Submission Link
CSE A	https://classroom.google.com/c/MjQxNTY3NDc5OTQ0/a/MjkyMDA5MzE1MjIz/details
CSE B	https://classroom.google.com/c/MjEyMTIzNDkwMjk4/a/Mjc0MDY4NzQ4MTU2/details
CSE C	https://classroom.google.com/u/1/w/MTI2MzQ5ODQ4NjYy/tc/MjkxNDQ2Nzk4MTky

Department & Section	Submission Link (Backlog)
CSE	https://classroom.google.com/c/MjkxNDQ2Nzk4Mjk1?cjc=po3mifq