DIGITAL LOGIC
(ECEN 2104)

Time Allotted: 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which of the following is not a valid octal number?
(a) 1101 (b) 740 (c) 970 (d) 220.

(ii) What is the Gray code word for the binary 101011?
(a) 101011 (b) 110101 (c) 011111 (d) 111110.

(iii) A full adder can be made out of
(a) Two half adders
(b) Two half adders and a NOT gate
(c) Two half adders and a OR gate
(d) Two half adders and a AND gate.

(iv) $(1111)_2$ in Grey code represents
(a) 9 (b) 15 (c) 10 (d) 16.

(v) If S=0, R=1 in a SR flip flop
(a) $Q_{n+1} = \bar{Q}_n$ (b) $Q_{n+1} = Q_n$
(c) $Q_{n+1} = 0$ (d) $Q_{n+1} = 1$.

(vi) The race around condition never occurs in Flip Flop
(a) J-K (b)T
(c) Master slave (d) None of these.

(vii) A three variable Karnaugh map has
(a) 16 minterms (b) 8 minterms
(c) 24minterms (d) 32 minterms.

(viii) The hexadecimal equivalent of the decimal number 115 is
(a) 72 (b) 73 (c) 70 (d) None of these.

(ix) 2's complement of binary number 0101 is
(a) 1011 (b)1101 (c)1110 (d)1001.

(x) A device which converts BCD to seven segment is called
(a) Encoder (b) Decoder
(c) Multiplexer (d) None of these.

Group – B

2. (a) Realise (i) $Y = A + BC\overline{D}$ using NAND gates and
(ii) $Y = (A+C)(A+\overline{D})(A+B+\overline{C})$ using NOR gates only.

(b) Apply DeMorgan's theorem to the given expression
$\overline{AB(CD + EF)}$

8 + 4 = 12

3. (a) Implement a 16-to-1 multiplexer using two 8-to-1 multiplexer.

(b) Implement the logic function $F = \sum m(1,2,5,6,7,8,10,12,13,15)$ using 8 input data selector MUX.

6 + 6 = 12

Group – C

4. Design a combinational circuit that will take 3 bit binary number as input and produce its equivalent Grey code. Write the truth table and draw the complete circuit diagram.

12

5. (a) Design an asynchronous Modulo 8 down counter using J-K flip flops.

(b) Design a 3-bit even parity generator and the corresponding 4 bit even parity checker circuit.

8 + 4 = 12

Group – D

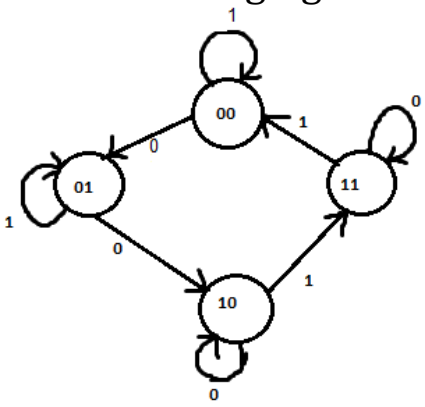
6. (a) A flip flop has a 10 ns delay from the time its CLK input goes from 1 to 0 to the time its output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip flops? What is the maximum frequency at which the counter can operate reliably?

(b) How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after the following count: (i) 1001100111 (ii) 0011111111.

(c) Draw the waveforms of a 10 flip flop ripple up counter.

4 + 4 + 4= 12

7. Design the clocked sequential circuit using JK flip flop, whose state diagram is given in the following figure.



12

Group – E

8. Construct a circuit using PROM type PLD that represents a function $Y=2X^2-X$, where X may vary from 0 to 7.

12

9. (a) Design a two input NOR gate using CMOS logic. Draw the switching diagram for all the possible input combinations.

(b) Draw and explain the general architecture of PLA structure.

6 + 6= 12

Department & Section	Submission Link (for Backlog)
CSE	https://classroom.google.com/c/MjkxMzkxNTUzMTIy?cjc=azj2z7w