B.TECH/AEIE/5TH SEM/AEIE 3102(BACKLOG)/2020

MICROPROCESSOR-ARCHITECTURE AND APPLICATIONS

(AEIE 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Address bus of 8085 μP is
(a) 8 bit unidirectional (b) 8 bit bi-directional
(c) 16 bit bi-directional (d) 16 bit unidirectional.

(ii) No of register pairs present in 8085 μP is
(a) 1 (b) 3 (c) 2 (d) 6.

(iii) Control signal used to de-multiplex address and data of 8085 μP is
(a)ALE (b) IO/ $\overline{M}$ (c) SID (d) READY.

(iv) Among the followings which interrupt has the lowest priority
(a)RST 5.5 (b) TRAP (c) RST 6.5 (d) RST 7.5.

(v) INX D is a _____ instruction
(a)1 byte (b)2 byte (c) 3 byte (d)4 byte.

(vi) In 8255 BSR mode of operation is for
(a)Port C only (b) Port A only
(c) Port A and Port B (d) Port A, Port B and Port .

(vii) 8259 IC is called
(a) Programmable peripheral interface
(b) Programmable interval timer
(c) Programmable interrupt controller
(d) USART.

(viii) In IO mapped I/O scheme, I/O devices are identified with ____ address
(a)8 bit (b) 10 bit (c) 16 bit (d) 24 bit.

(ix) The call location of RST 0 interrupt is
(a) 0000_H (b) 0008_H (c) 0024_H (d) 0034_H

(x) If the operating frequency of 8085 is 2 MHz, then the time required to execute ANA M instruction is-
(a) 3.5 μsec (b) 7 μsec (c)10 μsec (d) 14 μsec

Group – B

2.(a) Define programmable and non-programmable registers of 8085 μP with example.

(b) With suitable diagram discuss the function of ALE signal.

(c) Explain the function of following instructions (any two) –
(i) ADC B (ii) SHLD 9000_H (iii) DAD D

4+4+4=12

3.(a) Based on the size of the instruction classify the different instructions of 8085 μP with one suitable example.

(b) Define opcode and operand.

(c) Write an assembly language program to multiply two 8 bit numbers and store the result in memory locations.

(d) With suitable example explain the process of data storage in a stack memory.

3+2+5+2 = 12

Group – C

4. (a) Draw the timing diagram of ADD B instruction. Assume that the opcode of the instruction is XX_H and it is stored at memory location 9000_H. Also calculate the time required to execute the instruction where the operating frequency is 3 MHz.

(b) Write the name of different addressing modes of 8085 μP.

(7+2)+3 = 12

5.(a) What is the difference between vectored and non-vectored interrupt? What is the vector location of RST 7.5 interrupt?

(b) Draw and discuss RIM instruction format.

(c) Explain, if interrupt request is received through all the three lines- RST 7.5, RST6.5, RST5.5, which of the request will be served first after the execution of following instructions:

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MVI A,39H
SIM
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(d) With one suitable example explain the function of CALL and RET instruction.

(2+1)+3+3+3= 12

Group – D

6. Design an interface between 8085 µP and one 8KB RAM, one 16KB ROM memory chip. Calculate the address range of the memory chips.

10+2 = 12

7.(a) Interface one 7-segment display with 8085 µP, where the I/O port address is 80H. Write a program to display the last digit of your autonomy roll number.

(b) What is the limitation of memory mapped I/O technique?

(4+6)+2 = 12

Group – E

8.(a) Draw and discus the control word register (CWR) format of 8255 PPI in I/O mode.

(b) Draw the interfacing circuit to connect two LEDs to PC_0 and PC_7 line of 8255 PPI. Write an assembly language program for 8085 µP to periodically turn ON and OFF two LEDs by setting 8255 PPI in BSR mode.

(c) Write the control word value of 8255 PPI to set Port A as input in mode 1 and Port B as output in mode 1.

Write the 8085 µP instructions to load the above control word value in the CWR register. Assume Port A address is $F0_H$.

3+(3+3)+(1+2)= 12

9. Write short notes on (any three)

(i) Interfacing of stepper motor with 8085 µP through 8255 PPI
(ii) Internal architecture of 8254
(iii) ICWs of 8259
(iv) Internal architecture of 8251

4 ×3 = 12

Department & Section	Submission Link
AEIE	https://classroom.google.com/c/MjcxMDMzNDY3Mjk2/a/MjcxMDMzNDY3Mzcx/details