M.TECH/VLSI/1st SEM/VLSI 5102/2019

EMBEDDED SYSTEMS DESIGN (VLSI 5102)

Time Allotted : 3 hrs

Full Marks : 70

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and <u>any 5 (five)</u> from Group B to E, taking <u>at least one</u> from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A (Multiple Choice Type Questions)

- 1. Choose the correct alternative for the following: $10 \times 1 = 10$
 - (i) The locality of reference justifies the use of
 (a) Flash memory
 (b) Cache memory
 (c) Main memory
 (d) Virtual memory.
 - (ii) Primary agent responsible for correct working of an embedded system is (a) GPOS (b) RTOS (c) UNIX (d) WINDOWS.
 - (iii) Property which does not characterize an embedded system is

 (a) random output
 (b) real time output
 (c) low manufacturing cost
 (d) low power consumption.
 - (iv) An RTOS shall always have
 (a) time sensitive response
 (b) use of virtual memory
 (c) non-deterministic output
 (d) high interrupt latency.
 - (v) Three key technologies used for embedded systems are processor technology, _____ technology, and design technology.
 (a) system _____ (b) 10 _____ (c) seminary (c) seminar
 - (a) system (b) IC (c) gaming (d) computer
 - (vi) Which is not an embedded processor? (a) ARM 7 (b) ARM 9 (c) AMD 29050 (d) IBM 370.
 - (vii)The logic family with the fastest speed of execution is
(a) TTL(b) RTL(c) CMOS(d) ECL.
 - (viii) DMA can be used to transfer data directly between memory and a
 (a) peripheral unit
 (b) flipflop
 (c) counter
 (d) register.

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- (ix) How many separate address and data lines are needed for a RAM memory $16 \text{ K} \times 8$?
 - (a) 10 addresses, 16 data lines
 (b) 14 addresses, 8 data lines
 (c) 12 addresses, 16 data lines
 (d) 12 addresses, 12 data lines.
- (x) A Reaction timer may record the _____ elapsed between the turning an indicator lamp and the corresponding pressing of an response button.
 (a) picture
 (b) sound
 (c) image
 (d) time.

Group – B

- 2. (a) Which are the common characteristics of an embedded system?
 - (b) Which are the design-metrics normally optimized to meet the design challenges of an embedded system?
 - (c) Illustrate the basic steps for design of a custom Single Purpose Processor Design.

3 + 3 + 6 = 12

- 3. (a) Explain with examples what is a real time system? What are the differences between a RTOS and a GPOS?
 - (b) Explain Real Time classification as "hard", "firm" and "Soft" with examples. Where would one categorize the "Automatic Flight Control of Air plane".

6 + 6 = 12

Group – C

- 4. (a) What is Harvard Architecture? Explain briefly using a block diagram.
 - (b) Explain ARM Cortex 8 instruction Fetch Decode unit and Execute unit.
 - (c) A 4 stage pipeline system takes 20 ns to process a sub operation in each stage. The pipeline executes 100 tasks in sequence. What is the speed up ratio?

4 + 4 + 4 = 12

- 5. (a) Explain what is a Watch Dog Timer.
 - (b) Describe I2C BUS protocol.

6 + 6 = 12

Group – D

6. (a) Describe the main registers and the register bank operation of 8051 Controller. With example explain what are SFR registers.

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(b) List the I/O ports and their sizes for 8051, and briefly describe their functions.

6 + 6 = 12

- 7. (a) Explain briefly the ARM processor architecture and memory organization with block schematic.
 - (b) Explain the functions of Distributed Interrupt Controller for ARM 11 processors.
 - (c) What is a Snoop Control Unit in ARM 11?

(3+3)+4+2=12

Group – E

- 8. (a) Distinguish between SRAM and DRAM. Explain their reading and writing operation.
 - (b) An 8 bit DAC has a resolution of 15 mV/LSB. Determine (i) Full scale output voltage V_{fs} and (ii) Output voltage when the input digital word is "0001 0010".

6 + 6 = 12

- 9. (a) Why is DMA based I/O better than other I/O techniques?
 - (b) Distinguish between I/O mapped I/O and memory mapped I/O with proper examples.
 - (c) Explain the concepts of vectored and non-vectored interrupts.

4 + 4 + 4 = 12

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