DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Value of "Lambda" in 0.25 um Technology is
(a) 0.75 um (b) 0.5 um
(c) 1 um (d) 0.125 um.

(ii) The intermediate step between circuit design and fabrication in VLSI is
(a) logic design (b) physical design
(c) functional representation (d) system specification.

(iii) For a Standard Cell Layout
(a) width is fixed (b) height is fixed
(c) both height and width are fixed (d) none of (a), (b) and (c).

(iv) Memory Design is normally done using the method below
(a) Full custom (b) Std Cell based Semi Custom
(c) Gate array (d) FPGA.

(v) With increase of V_{dd}, the Delay of an CMOS inverter
(a) increases (b) decreases
(c) remains Same (d) becomes infinite.

(vi) Minimum number of transistors in CMOS logic Y = AB + CD is
(a) 12 (b) 6
(c) 8 (d) 10.

(vii) Latch up occurs for CMOS as
(a) CMOS invariably picks up stray signal
(b) unavoidable existence of npn, pnp transistors embedded in CMOS
(c) absence of parasitic effect
(d) CMOS has low power dissipation.

(viii) Stick diagram represents
(a) Logic (b) Circuit
(c) Layout (d) Architecture.

(ix) LUT belongs to below one of the types of circuits
(a) Gate Array (b) CPLD
(c) PLA (d) FPGA.

(x) KL algorithm is related to
(a) routing (b) partitioning
(c) logic synthesis (d) high level synthesis.

Group – B

2. (a) Draw circuit diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw circuit diagram of a negative edge triggered D-Flip Flop using D-Latch.

(c) Draw circuit diagram of 2 input XOR gate using CMOS logic.

(d) Draw circuit diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

3 + 3 + 3 + 3 = 12

3. (a) Draw layout of CMOS inverter using Standard Cell Layout Topology and show all the layers.

(b) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule" ?

(c) Draw the schematic and Stick Diagram of 2 input NOR gate.

4 + 3 + 5 =12

Group – C

4. (a) Draw Y chart for VLSI design.

(b) Draw flow diagram of VLSI design cycle.

(c) Draw flow diagram of front end design flow.

(d) Write VHDL behavioural model for a D –Flip Flop.

3 + 3 + 3 + 3 = 12

5. (a) Draw VTC curve for CMOS inverter and show various region.

(b) Draw Domino implementation of 3 input NOR gate.

(c) Implement f = A.B boolean logic using Transmission Gate.

3 + 4 + 5 = 12

Group – D

6. Write short notes on topic below
   (i) FPGA.
   (ii) Finite State Machine.
   (iii) Technology Library Mapping for Logic Synthesis.

4 + 4 + 4 = 12

7. (a) Draw flow diagram of Physical Layout Automation.

   (b) For floor-planning problem, what are inputs, outputs and objective (Cost) function ?

   (c) Explain Lee Algorithm of Maze Routing.

4 + 4 + 4 = 12

Group – E

8. (a) What are key limitations of pseudo-NMOS logic family?

   (b) Why CMOS transmission gate is used instead of NMOS pass transistor logic.

   (c) Draw BDD diagram for function f = abc + ab'c + a'bc' + a'b'c' using ordering of a $\leq$ b$\leq$ c.

   (d) Draw circuit diagram of 12 input OR gate using domino circuit.

2 + 2 + 4 + 4 = 12

9. Write short notes on the following:
   (i) Left Edge Algorithm for detailed routing.
   (ii) Global routing using Steiner tree.
   (iii) I-V characteristics of MOS transistor.

4 + 4 + 4 = 12