(iii) What are the practical limitations preventing the growth of the super-pipeline degree n?

(4+ 4 + 4) = 12

Group – E

8. (a) Describe a superscalar RISC processor architecture consisting of an integer unit and a floating-point unit with diagram.

(b) Write down the advantages and disadvantages of Centralized shared-memory architecture and distributed shared-memory architecture.

6 + (3 + 3) = 12

9. (a) Describe the Omega, Baseline and Crossbar interconnection network with diagram.

(b) State the factors which affect the performance of an interconnection network.

(3+3+3) + 3 = 12

COMPUTER ARCHITECTURE
(INFO 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The pipelining process is also called as _____.
(a) Superscalar operation (b) Assembly line operation
(c) Von Neumann cycle (d) none of the mentioned

(ii) The fetch and execution cycles are interleaved with the help of _____.
(a) modification in processor architecture (b) Clock
(c) Special unit (d) Control unit

(iii) When the processor executes multiple instructions at a time it is said to use _____.
(a) Single issue (b) Multiplicity (c) Visualization (d) Multiple issues

(iv) The situation wherein the data of operands are not available is called _____.
(a) Data hazard (b) Stock (c) Deadlock (d) Structural hazard

(v) The _____ plays a very vital role in case of super scalar processors.
(a) Compilers (b) Motherboard (c) Memory (d) Peripherals

(vi) The CISC stands for _____.
(a) Computer Instruction Set Compliment
(b) Complete Instruction Set Compliment
(c) Computer Indexed Set Components
(d) Complex Instruction Set Computer

(vii) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order (c) Out of order (d) None of the mentioned

(viii) If a system is 64 bit machine, then the length of each word will be _____.
(a) 12 bytes (b)16 bytes (c)4 bytes (d) 8 bytes

(ix) The step where in the results stored in the temporary register is transferred into the permanent register is called as _____.
(a) Final step (b) Commitment step
(c) Last step (d) Inception step

(x) During the transfer of data between the processor and memory we use ____.
(a)TLB (b)Buffers (c) Cache (d) none of the above

Group – B

2. (a) Explain how do instruction set, compiler technology, CPU implementation and control, and cache and memory hierarchy affect the CPU performance and justify the effects in terms of program length, clock rate, and effective CPI.

(b) A workstation uses a 15 MHz processor with a claimed 10-MIPS rating to execute a given program mix. Assume a one-cycle delay for each memory access.

(i) What is the effective CPI of this computer?

(ii) Suppose the processor is being upgraded with a 30 MHz clock. However, the speed of the memory subsystem remains unchanged, and consequently two clock cycles are needed per memory access. If 30% of the instruction require one memory access and another 5% require two memory access per instruction, what is the performance of the upgraded processor with a compatible instruction set and equal instruction counts in the given program mix?

(2 + 2+ 2) + (3 + 3) = 12

3. (a) Consider the five-stage pipelined processor specified by the following reservation table.

1	2	3	4	5	6	
X					X	S1
	X			X		S2
		X				S3
			X			S4
	X				X	S5

(i) List the set of forbidden latencies and the collision vector.
(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.

(iii) List all the simple cycles from the state diagram.
(iv) Identify the greedy cycles among the simple cycles.
(v) What is the minimum average latency (MAL) of this pipeline.

(b) Consider the execution of a program of 15000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence are ignored. What are the efficiency and throughput of this pipelined processor?

(2+ 2+ 2 + 2 + 2) + 2 = 12

Group – C

4. (a) What is locality of reference? Classify cache memory and define split cache.

(b) A memory system consists of cache, main and virtual memory. Hit rate in cache is 87% and hit rate in RAM is 89%. Calculate the average memory access time if it takes 2 cycles to access the cache, 50 cycles to fetch memory line and 2000 cycles to access virtual memory.

(c) Classify all types of the memory in the computer system considering the size, cost and efficiency.

(2 + 2) + 6 + 2 = 12

5. (a) What is TLB and PMT, explain with example. What is Belady's Anomaly?

(b) Consider the following page references and calculate the hit and miss ratio applying FIFO and LRU algorithm (let, cache memory has 4 page frames).
3 1 2 3 1 2 4 2 1 3 1 5

(3 + 3) + 6 = 12

Group – D

6. (a) State the design parameters for pipeline processors.

(b) Discuss the structure of superscalar pipelines, the data dependence problem, the factors causing pipeline stalling and multiinstruction-issuing mechanisms (in-order issue and out-of-order issue) in the context of superscalar pipeline design.

2 + (4 + 2 +2 + 2) = 12

7. This problem compares the performance of super-pipelined superscalar processor of degree (m, n) with that of a base scalar processor of degree(1,1). Analyze the following speedup expression for the below mentioned limiting cases:
$S(m, n) = m*n(k+N-1)/ m*n*k + N-m$ where, N=number of independent instructions and k= number of pipeline stages

(i) Within the range $1 <= m <= 4$ and $1 <= n <= 6$, what is the optimal number of pipeline stages that would maximize the speedup S(m, n)?
(ii) What are the practical limitations preventing the growth of the superscalar degree m?