DIGITAL SYSTEMS DESIGN
(ECEN 2002)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A decoder with enable input can be used as
(a) Encoder (b) Parity Generator
(c) Multiplexer (d) Demultiplexer.

(ii) $(1\ AF)_{16}$ =
(a) $(567)_8$ (b) $(576)_8$
(c) $(657)_8$ (d) $(557)_8$.

(iii) The number of full adders required to construct an m-bit parallel adder is
(a) m/2 (b) m-2
(c) m (d) m+1.

(iv) Excess 3 code representation of $(19)_{10}$ is
(a) 10011 (b) 00011001
(c) 01001100 (d) 11000100.

(v) The simplified form of the Boolean expression (X+Y+XY)(X+Z) is
(a) X+Y+Z (b) XY+YZ
(c) X+YZ (d) XZ+Y.

(vi) Which of the following flip-flop is used as a latch?
(a) J-K flip-flop (b) Master-Slave flip-flop
(c) T flip-flop (d) D flip-flop.

(vii) A (32×10) ROM contain a decoder of size
(a) 32×32 (b) 5×32
(c) 32×10 (d) 10×32.

(viii) Resolution of n-bit DAC is given by
(a) $1/(2^n-1)$ (b) $1/2^n$
(c) $1/(2^n+1)$ (d) $1/2^{-n}$.

(ix) A 4-stage ripple counter counts up to
(a) 12 (b) 15
(c) 11 (d) 4.

(x) The slowest ADC is
(a) counter type (b) flash type
(c) successive approximation type (d) dual slope type.

Group – B

2. (a) Simplify the Boolean function by using K-map:
$F= \sum m(0, 1, 2, 8, 10, 11, 14, 15)+ \sum d(3,13)$.

(b) Prove that $F=\sum m(1,2,3,4)= \prod M(0,5,6,7)$.

(c) (i) Convert 756.603_8 to hex.
(ii) Convert $B9F.AE_{16}$ to octal.

4 + 4 + (2 + 2) = 12

3. (a) Simplify the following function in SOP form using Quine MC-Cluskey method:
$F(A, B, C, D)=\sum m(0,1,4,7,9,11,13,15) + \sum d(3,5)$.

(b) Realize the X-OR function using (i) AOI logic (ii) NAND logic.

8 + 4 = 12

Group – C

4. (a) Design 16 : 1 MUX using five 4 : 1 MUX.

(b) Design full substractor circuit using 4 : 1 MUX and necessary logic gates.

(c) What are the difference between Decoder and Demultiplexer?

5 + 5 + 2 = 12

5. (a) Implement the function F(a,b,c) = $ab + \bar{b}c$ using 4 : 1 MUX.

(b) Construct two bit comparator using basic logic gates.

(c) Give the logic implementation of a 8 × 4 bit ROM using a decoder of a suitable size.

5 + 4 + 3 = 12

Group – D

6. (a) What do you mean by Race-around condition of a flip-flop? How can it be overcome?

(b) What is the main difference between a latch and a flip-flop?

(c) Convert D flip-flop to SR flip-flop.

(2 + 1) + 3 + 6 = 12

7. (a) Design a counter that goes through states 3, 4, 6,7and 3 states using JK flip-flops.

   (b) A binary ripple counter is required to count up to 16383_{10} .How many FFs are required? If the clock frequency is 8.192 MHz, what is the frequency at the output of the MSB?

8 + 4 = 12

Group – E

8. (a) With the help of necessary circuit diagram, explain the operation of dual slope ADC.

   (b) What are the advantages and disadvantages of the Flash Type A/D converter?

   (c) Design a 2-input NAND gate using CMOS inverter.

6 + 2 + 4 = 12

9. Write short notes on any three of the following. **(4 × 3) =12**
   (i) Parallel In Serial Out shift register
   (ii) CMOS
   (iii) TTL
   (iv) Priority Encoder
   (v) Master Slave flip flop.