VLSI DESIGN AUTOMATION
(ECEN 4181)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) For Sub Micron Technology L_{gate} (Channel Length) is
(a) > 1 um (b) < 100 nm (c) > 100 nm (d) none of these.

(ii) Output of physical design is
(a) Schematic (b) Layout
(c) Logical Model (d) RTL.

(iii) The HDL used for industrial purpose is
(a) SPECTRA (b) MATLAB
(c) VERILOG (d) PSPICE.

(iv) The enhancement NMOS type Transistor is basically termed as normally 'OFF" Transistor which becomes "ON" only with
(a) large positive gate voltage
(b) large negative gate voltage
(c) large positive drain voltage
(d) large negative drain voltage.

(v) MOS Transistor has below number of terminals
(a) 1 (b) 2 (c) 3 (d) 4.

(vi) If both the transistors are in saturation, then they act as?
(a) Current source (b) Voltage source
(c) Divider (d) Buffer.

(vii) Which of the following is the fundamental architecture block or element of a target PLD?
(a) System partitioning
(b) Pre - layout simulation
(c) Logic cell
(d) Post - layout simulation.

(viii) Which of the following method is normally used for finite state machine?
(a) Full Custom (b) Std Cell based Semi Custom
(c) FPGA (d) Gate Array.

(ix) With decrease of CL, the Delay of an CMOS inverter?
(a) Increases (b) Decreases
(c) Remains same (d) Becomes infinite.

(x) Which of the following represents the stick diagram?
(a)Logic (b) Circuit (c) Layout (d) Architecture.

Group – B

2. (a) What is issue related to NMOS based Inverter Design?

(b) How the issue is fixed using CMOS based Inverter?

6 + 6 = 12

3. (a) Draw schematic diagram of CMOS gate which represents function f = (D + E)$_{.}$ (B + C)! (! Means Bar).

(b) Draw stick diagram of CMOS gate which represents function f = (A $_{.}$ B) + C! (! Means Bar).

(c) With the help of a proper example, explain the steps involved in Euler's algorithm.

4 + 4 + 4 =12

Group – C

4.(a) What is function of a Latch?

(b) Implement Latch using Transmission Gate (TG) Logic.

(c) What is function of a Flip-Flop?

(d) How Flip Flop can be implemented using Latch?

3+ 3+ 3+ 3 = 12

5. (a) What do you mean by physical design and also mention the need of physical design in VLSI?

(b) Discuss the various steps required for physical design.

(c) Define Moore's law.

(3 +3)+ 4 + 2 = 12

Group – D

6. (a) For floorplanning problem, what are inputs, outputs and Objective (Cost) function ?

(b) Write problem formulation of Global Routing using Steiner Tree.

6 + 6 = 12

7. (a) Define scheduling and mention its basic objective?

(b) Explain in details about as soon as possible (ASAP) and as late as possible (ALAP) algorithm?

6 + 6 =12

Group – E

8. (a) Write Verilog code of Behavioural Modelling of a 3 input NOR gate.

(b) Draw Flow Diagram of High Level Synthesis.

6 + 6 = 12

9. Write short notes on the following topics:
(a) KL algorithm.
(b) Example of OBDD and ROBDD.

6 + 6 =12