Group – E

8. (a) Draw and explain the small signal model of the push – pull amplifier and calculate its small signal voltage gain.

   (b) Evaluate the differential voltage gain of a resistive load differential amplifier circuit.

   (c) In the circuit of Fig. 2, M2 is twice as wide as M1. Calculate the small signal gain if the bias values of Vin_1 and Vin_2 are equal.

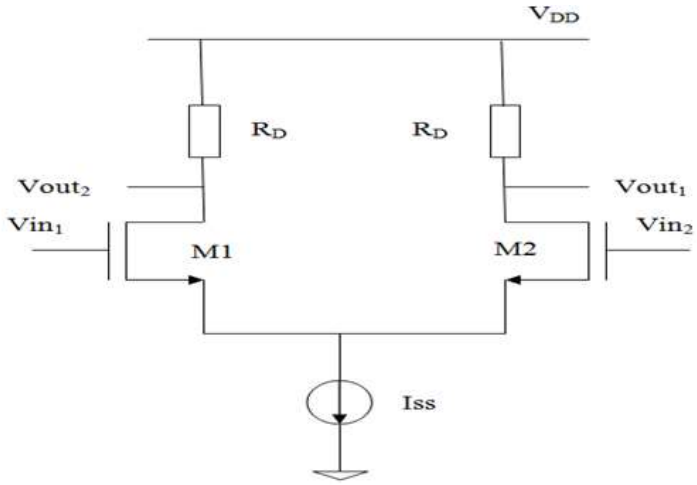

Fig. 2

4 + 5 + 3 = 12

9. (a) Draw the circuit of common source MOSFET amplifier.

   (b) Draw the circuit of differential amplifier with active load.

   (c) Draw the circuit of switched capacitor integrator.

4 + 4 + 4 = 12

MICROELECTRONICS & ANALOG VLSI DESIGN (ECEN 3103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) At the threshold inversion point, space charge width reaches its
   (a) Minimum (b) Maximum
   (c) $x_{dT} = N_a/\varphi_{fp}$ (d) $x_{dT} = 2N_a/\varphi_{fp}$

   (ii) Ideal MOSFET can be considered as a constant current source when operated in
   (a) triode region (b) deep triode region
   (c) saturation region (d) none of the above.

   (iii) For low frequency operation, MOS capacitance in the strong inversion region is equivalent to the
   (a) insulator capacitance
   (b) depletion layer capacitance added in series with insulator capacitance
   (c) depletion layer capacitance
   (d) depletion layer capacitance added in parallel with insulator capacitance.

   (iv) The channel resistance (r_0) of the MOSFET is related with the channel length modulation parameter (λ)
   (a) $r_0 \alpha \lambda^{-1}$ (b) $r_0 \alpha \lambda^{-1/2}$
   (c) $r_0 \alpha \lambda$ (d) $r_0 \alpha \lambda^{1/2}$

   (v) The gate-to-channel capacitance of the MOSFET is given as
   (a) $C_{GC}=W_{eff}(L+L_D)C_{OX}$ (b) $C_{GC}=W_{eff}LC_{OX}$
   (c) $C_{GC}=W_{eff}(L-L_D)C_{OX}$ (d) $C_{GC}=W_{eff}(L-2L_D)C_{OX}$.

   (vi) Most popular scaling technique in today's nanotechnology is
   (a) Constant Voltage Scaling (b) Constant Field Scaling
   (c) Constant Energy Scaling (d) Constant Charge Scaling.

(vii) The performance of a current sink / source circuit can be improved by
(a) reducing V_{MIN} and output resistance
(b) increasing V_{MIN} and output resistance
(c) reducing V_{MIN} and increasing output resistance
(d) increasing V_{MIN} and reducing output resistance.

(viii) DIBL can be mitigated by
(a) increasing the doping concentration
(b) making the junction depth shallow
(c) none of the above
(d) both (a) & (b).

(ix) Switched capacitor circuit realizes
(a) Capacitance (b) Resistance
(c) Inductance (d) Current Source.

(x) 0.7 technology scaling enables layout area scaling of
(a) 0.7 (b) 0.5
(c) 0.45 (d) 0.65.

Group – B

2. (a) Derive the expression for metal–semiconductor work function difference of the MOS structure with the help of energy band diagram.

(b) Consider an n^+ Poly Silicon gate and *p-type* silicon substrate doped to $N_a=3\times10^{16}\ cm^{-3}$. Assume, $Q_{ss}'=10^{11}\ cm^{-2}$, $\varepsilon_{r(semiconductor)}=11.7$, $\varepsilon_{r(oxide)}=3.9$, $n_i=1.5\times10^{10}\ cm^{-3}$, $V_t=0.026\ V$ and $\varphi_{ms}=-1.13V$. Determine the oxide thickness such that $V_{TN}=+0.65V$. All the symbols have their usual significance.

6 + 6 = 12

3. (a) What are Constant Voltage Scaling and Constant Field Scaling?

(b) Which scaling is more popular and why ?

(c) Explain the several Short Channel Effects observed in a scaled MOSFETs.

4 + 3 + 5 =12

Group – C

4. (a) Explain photo lithography.

(b) Briefly describe the diffusion process.

(c) Distinguish between dry etching and wet etching. Briefly explain electromigration.

4 + 4 + 4 = 12

5. (a) Briefly describe the n-well fabrication process.

(b) A proximity printer operates with a 20 μm mask to wafer gap and a wavelength of 250 nm. Find the minimum linewidth that can be obtained.

10 + 2 = 12

Group – D

6. (a) What are the design steps for analog VLSI flow?

(b) Draw large signal models for NMOS.

(c) What is transconductance and on what parameters it depends?

3 + 4 + 5 = 12

7. (a) Explain the principle of operation of cascode current sink circuit. Explain quantitatively the principle used in biasing MOS devices for reduction of V_{MIN} in the current sink circuit. Also, show how V_{MIN} is reduced in high – swing cascode circuit.

(b)

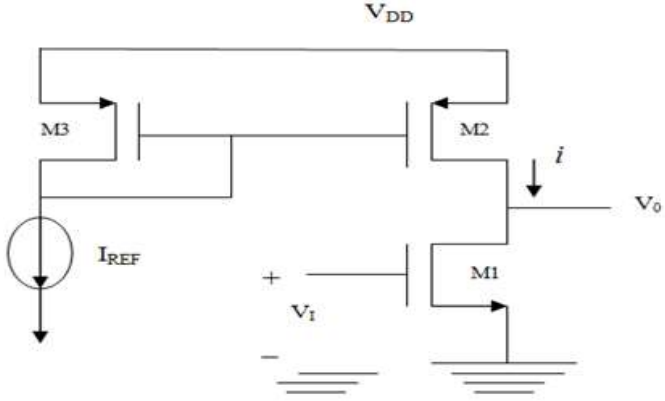

Fig. 1

Consider the common–source amplifier (Fig. 1) for the case $V_{DD}=3\ V$, $V_{tn}=|V_{tp}|=0.6\ V$, $\mu_nC_{OX}=200\ \mu A/V^2$, and $\mu_pC_{OX}=65\ \mu A/V^2$. For all transistors, $L=0.4\ \mu m$, and $W=4\ \mu m$. Also, $V_{An}=20\ V$, $|V_{Ap}|$ = 10 V, and $I_{REF}=100\ \mu A$. Find the small signal voltage gain.

(3 + 3 + 3) + 3 = 12