DIGITAL LOGIC DESIGN
(MCAP 1101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) What is the binary equivalent of the decimal number 368?
(a) 101110000 (b) 110110000
(c) 111010000 (d) 111100000.

(ii) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) Sign-magnitude (b) 1's complement
(c) 2's complement (d) 9's complement.

(iii) The number of control lines for a 8 – to – 1 multiplexer are
(a) 2 (b) 3 (c) 4 (d) 5.

(iv) The Gray code for decimal number 6 is equivalent to
(a) 1100 (b) 1001 (c) 0101 (d) 0110.

(v) EPROM contents can be erased by exposing it to
(a) ultraviolet rays (b) infrared rays
(c) burst of microwaves (d) intense heat radiations.

(vi) Which of the memory is volatile memory?
(a) ROM (b) RAM (c) PROM (d) EEPROM.

(vii) The device which changes from serial data to parallel data is
(a) counter (b) multiplexer
(c) demultiplexer (d) flip-flop.

(viii) A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be
(a) 15 ns (b) 30 ns (c) 45 ns (d) 60 ns.

(ix) The output of a JK flipflop with asynchronous preset and clear inputs is '1'. The output can be changed to '0' with one of the following conditions.
(a) By applying J = 0, K = 0 and using a clock
(b) By applying J = 1, K = 0 and using the clock
(c) By applying J = 1, K = 1 and using the clock
(d) By applying a synchronous preset input.

(x) When the set of input data to an even parity generator is 0111, the output will be
(a) 1 (b) 0
(c) Unpredictable (d) depends on the previous input.

Group – B

2. (a) Convert the decimal number 54689 to its hexadecimal equivalent number.

(b) What is the Gray equivalent of $(25)_{10}$?

(c) Using 7's complement and 8's complement, obtain the difference: $456_8 - 173_8$.

4 + 3 + 5 = 12

3. (a) Convert $(156.25)_{10}$ to octal.

(b) Using 15's complement and 16's complement, obtain the difference: $ECFD_{16} – A4AE_{16}$.

(c) Determine the binary number represented by the following decimal number: 15.25.

4 + 5 + 3 = 12

Group – C

4. (a) Simplify and draw the logic diagram for the given expression F = (ABC)' + (AB)'C + A'BC' + A(BC)'AB'C.

(b) Why do 11 come before 10 in the K-map?

(c) Show how a two input X-OR gate can be constructed only from 2 input NAND gates.

7 + 2 + 3 = 12

5. (a) Simplify the following expression into sum of products using Karnaugh map F(A, B, C, D) = (1, 3, 4, 5, 6, 7, 9, 12, 13).

(b) Simplify the Boolean expression F = C(B + C)(A + B + C).

7 + 5 = 12

Group – D

6. (a) Design (4:1) multiplexer using (2:1) multiplexers.

   (b) Design a 8 to 1 multiplexer by using the four variable function given by $F(A, B, C, D) = \sum m(0, 1, 3, 6, 7, 9, 15)$.

5 + 7 = 12

7. (a) Show how a full adder can be converted to a full subtractor with the addition of just one inverter with the full adder circuit.

   (b) Design a half adder circuit using minimum number of 2-input NOR gates only. Write down the truth table and Boolean function.

7 + 5 = 12

Group – E

8. (a) Explain the working principle of SR flip flop with suitable example.

   (b) Why a gated D latch is called 'transparent' latch?

   (c) What is the difference between a latch and edge triggered flip-flop?

6 + 3 + 3 = 12

9. (a) What is difference between synchronous counter and asynchronous counter?

   (b) What is a shift register? Can a shift register be used as a counter? If yes, explain how?

   (c) With relevant diagram explain the working of master-slave SR flip flop.

3 + 3 + 6 = 12