9. (a) What is the difference between a latch and an edge triggered flip-flop?

(b) Design a S-R flip flop using NAND gate and explain its working.

(c) Convert an S-R flip-flop to a J-K flip flop.

2 + 5 + 5 = 12

ANALOG & DIGITAL ELECTRONIC CIRCUITS
(ELEC 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The output of an integrator circuit with square wave input is
(a) triangular wave (b) impulse
(c) parabola (d) step.

(ii) The bandwidth of an ideal op amp is
(a) infinity (b) 1 MHz (c) 0 Hz (d) 10 Hz.

(iii) The output resistance of an ideal op amp is
(a) Zero (b) 75Ω (c) infinity (d) 1MΩ.

(iv) Which is the necessary condition of gain while designing Wien bridge oscillator to ensure the sustained oscillations?
(a) $A \geq 3$ (b) $A \geq 2$ (c) $A \geq 29$ (d) $A \geq 1$.

(v) An ideal regulated power supply should have regulation equal to
(a) zero (b) 50% (c) 100% (d) 25%.

(vi) The Boolean expression $\bar{A}B\bar{C}\bar{D}$ is a
(a) a sum term (b) a product term
(c) a literal term (d) always 1.

(vii) A 4-bit parallel adder can add
(a) two 4-bit binary number
(b) two 2-bit binary number
(c) four bits at a time
(d) four bits in sequence.

(viii) Why is a Demultiplexer called a data distributor?
(a) The input will be distributed to one of the outputs
(b) One of the inputs will be selected for the output
(c) The output will be distributed to one of the inputs
(d) Single input gives single output.

(ix) In an S-R latch built from NOR gates, which condition is not allowed
(a) S = 0, R = 0 (b) S = 0, R = 1
(c) S = 1, R = 0 (d) S = 1, R = 1.

(x) If Q = 0, the output is said to be
(a) set (b) reset
(c) previous state (d) current state.

Group – B

2. (a) Realise the following linear differential equation using minimum number of Op-amp:

$$\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + 3y = 1$$

(b) Derive the expression of voltage gain and input resistance for a voltage shunt feedback amplifier.

6 + 6 = 12

3. (a) Design an Op-amp based subtractor circuit with 2 inputs V_1 and V_2 such that the output $V_0 = 3V_2 - 5V_1$

(b) Draw the circuit diagram of integrator using Op-amp. Deduce the expression for output voltage. Mention the problems in the circuit and how do we modify the circuit to overcome them?

(c) Define slew rate and common mode rejection ratio.

4 + 6 + 2 = 12

Group – C

4. (a) Explain with the help of a neat circuit diagram the principle of operation of an astable multivibrator using Op-amp. Sketch the output voltage and the capacitor voltage waveforms. Derive the expression of time period.

(b) Why do we connect the RESET pin of IC555 timer to $+V_{cc}$?

10 + 2 = 12

5. (a) Draw a neat diagram of a zero crossing detector circuit. Explain its principle of operation. Draw the output waveform for a 15V p-p sine wave input.

(b) Using 7805 C voltage regulator design a current source that will deliver 0.2 A current to a 48 Ω, 10 W load.

(c) Design a phase shift oscillator so that frequency of oscillation is equal to 200 Hz.

4 + 4 + 4 = 12

Group – D

6. (a) Design an XOR gate using a NAND gate.

(b) Simplify the Boolean expression using Karnaugh map technique:
$F(A,B,C,D) = \sum_m(0,7,8,9,10,12) + \sum d(2,5,13)$
Also implement the circuit using suitable logic gates.

(c) Design a full adder using two half adders and an external gate if necessary.

2 + 5 + 5 = 12

7. (a) Write a short note on Multiplexer.

(b) Implement the following Boolean expression using a (8 × 1) MUX:
$F(A,B,C,D) = \sum_m(0,1,3,4,8,9,13,15)$

(c) Design a (16 × 1) MUX using (8 × 1) MUX and external gate.

2 + 5 + 5 = 12

Group – E

8. (a) What is the difference between an asynchronous and a synchronous counter?

(b) Design a 3 bit asynchronous Up Counter using JK flip flop and explain its working. Draw the timing diagram.

(c) Design a 3 bit shift register using D flip flop and explain its operation for right shift mode.

2 + 5 + 5 = 12