7. (a) Briefly explain the butterfly network.

(b) What is the significance of interconnection network in multiprocessor architecture?

(c) Write down algorithm for odd- even transposition sort and explain it using a set of data.

4 + 3 +5 = 12

Group – E

8. (a) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts :

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program.

(b) (i) Mention two important differences between control flow and data flow architecture.

(ii) Draw a data flow graph to find out the approximate value of sin(x), using the following formula

$\sin(x) = x - x^3/6 + x^5/120 - x^7/5040$

5 + (2 + 5) = 12

9. (a) Calculate the speedup factor for superscalar architecture and superpipelined architecture.

(b) Explain the concept of VLIW architecture, highlighting how it is different from instruction level parallelism.

(c) Suppose that in an MIMD system, there are 20 processors. Each has its own cache. Suppose two processors each caches a single shared variable X. How many messages are sent across the system for maintaining cache coherency of X if 1) Snooping protocol is used? 2) If a Centralized Directory Based Protocol is used? Explain your answer.

5 +3 + 4 = 12

COMPUTER ARCHITECTURE
(CSEN 3104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The speedup of a k-stage pipelined processor to complete n tasks, compared to a non-pipelined processor is
(a) n / (k+n -1) (b) n / (k*n -1)
(c) n*k / (k+n-1) (d) n*k / (k*n -1).

(ii) For two instructions I and J, WAW Hazard will occur, if
(a) $R(I) \cap D(J) \neq \Phi$ (b) $D(I) \cap R(J) \neq \Phi$
(c) $R(I) \cap R(J) \neq \Phi$ (d) None of (a),(b),(c).

(iii) How many 4 × 3 crossbar switches are required to implement a $4^2 \times 3^2$ Delta Network?
(a) 12 (b) 7 (c) 14 (d) 9.

(iv) For multiplication of two matrices A (3 × 4) and B (4 × 6) using parallel algorithms in SIMD computer, the advantage in the computation time, compared to that in SISD computer is of the order of
(a) 3 times (b) 4 times (c) 6 times (d) 12 times.

(v) The prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) None of (a),(b),(c).

(vi) For an n × n array of processing elements, the M(n,n) sort algorithm can be done in time proportional to
(a) O(n) (b) $O(n^2)$ (c) O(logn) (d) O(nlogn).

(vii) Which of the following is an example of 2-dimensional topologies in static network?
(a) Mesh (b) $3c^3$ network
(c) Linear Array (d) None of (a),(b),(c)..

(viii) Memory access in RISC architecture is limited to instructions
(a) CALL and RET (b) PUSH and POP
(c) STA and LDA (d) MOV and JMP.

(ix) Which of the following types of instructions are useful in handling sparse matrices in vector processing applications?
(a) Vector- scalar instruction
(b) Vector – memory instruction
(c) Masking instruction
(d) Scatter – gather instruction.

(x) Shuffle function $S(a_{n-1} \ldots a_1 a_0)$ is mathematically given by
(a) $a_{n-2}a_{n-3} \ldots\ldots a_1 a_0 a_{n-1}$ (b) $a'_{n-1}a_{n-2} \ldots\ldots a_1\, a_0$
(c) $a_0 a_{n-1}a_{n-2} \ldots\ldots a_1$ (d) $a_{n-1}a_{n-2} \ldots\ldots a_1\, a'_0$
where the symbol ' denotes complement

Group – B

2. (a) How can hazard occur in executing the following set of instructions?
I1: MOV R1,A ; [A] <- (R1)
I2: ADD R2,R3; R3 <- (R3) + (R2)
I3: SUB R4,R5; R5 <- (R4) – (R5)
I4: NOP
All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.

(b) Differentiate between Von Neuman and Harvard Architecture, explain with schematic diagram.

(c) Draw the tree that results in multiplying two 5 bit numbers using CSA's.

4 + 4 + 4 = 12

3. Consider the following reservation table. Write down the forbidden latencies, permissible latencies and initial collision vector. Draw the state diagram for scheduling the pipeline. Find out simple cycles, greedy cycle and MAL. What are the upper and lower bounds on MAL?

	1	2	3	4	5
Stage 1	X				X
Stage 2		X	X		
Stage 3				X	

(3 + 4 + 3 + 2) = 12

Group – C

4. (a) Illustrate the necessity of data routing in an array processor by showing the execution details to compute

$$S(k) = \sum_{i=0}^{k} A_i \qquad \text{for } k = 0, 1, \ldots\ldots, (n-1)$$

(b) Explain Strip Mining and vector chaining using examples.

(c) Draw a 3-D cube showing the binary addresses of the PEs at all the vertices. Show the recirculating cube network for all possible routing functions.

5 + 4 + (1 + 2) =12

5. (a) Explain the multistage implementation of cube network with a suitable diagram.

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node 101 simultaneously in a 8 × 8 Omega network. Does blocking exist in this case?

(c) You have the following Instruction Stream coming into a chained Vector Processor
Load VR , A[3:0]
Add VR , #1
Mul VR , #2
Store A[3:0] , VR
A is a vector if length 4. VR is a Vector register.
Show how the above code is executed in a Vector processor with four pipeline stages (Load / Add / Multiply and Store).

4 + (2+2+1) + 3 = 12

Group – D

6. (a) Show how the following two matrices can be multiplied using SIMD matrix multiplication algorithm?

$$\begin{bmatrix}1 & 2\\ 4 & 5\end{bmatrix}\begin{bmatrix}4 & 7\\ 7 & 6\end{bmatrix}$$

(b) Draw 3^2 X 4^2 Delta network.

(c) Consider the following program: (assume Opcode <srec>,<dest> format):

Add R3, R2
Sub R3,R4
Add R2,R1
Mov R1,[R4] ; writes to memory location
;pointed to by R4
Jnz R1, ThisPlace
: : : : : :
ThisPlace: <some code>

Assuming a delay slot value of 3, rewrite the code to exploit the Delayed Branching mechanism. Explain briefly how performance is improved because of application of the above technique.

4 + 3 +5 = 12