MICROPROCESSOR - ARCHITECTURE AND APPLICATIONS
(AEIE 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Program Counter (PC) register present in 8085 µP is a ____ register.
(a) 4 bit (b) 8 bit (c) 32 bit (d) 16 bit

(ii) LDAX B is a ____ instruction.
(a) 1 byte (b) 2 byte (c) 3 byte (d) 4 byte

(iii) Length of MOV A, M instruction is
(a) 1 byte (b) 2 byte (c) 3 byte (d) 4 byte.

(iv) If the crystal frequency connected with 8085 is 4 MHz, then the time required to execute an instruction with 13T states is
(a) 15 µsec (b) 10 µsec (c) 6.5 µsec (d) None of these.

(v) Program Status Word (PSW) of 8085 µP is ___.
(a) 8 bit (b) 16 bit (c) 4 bit (d) 24 bit

(vi) If CWR address of 8255 connected to 8085 is 80_H, then address for Port B is
(a) $7F_H$ (b) 81_H (c) $7E_H$ (d) 82_H.

(vii) 8251 IC is called
(a) Programmable peripheral interface
(b) Programmable interval timer
(c) Programmable interrupt controller
(d) USART.

(viii) Mode 2 of 8253 is
(a) Square wave generator (b) Rate generator
(c) Software trigger strobe (d) Hardware trigger strobe.

(ix) In JNZ 8000_H instruction program execution will be shifted to 8000_H memory location when
(a) CY = 1 (b) CY = 0 (c) Z = 1 (d) Z = 0.

(x) In 8085 µP top of the stack memory address is pointed by which register?
(a) PC (b) SP (c) HL pair (d) W and Z.

Group – B

2. (a) Draw and discuss the flag register of 8085 µP.

(b) With one suitable instruction discuss the function of SP register.

(c) Discuss the function of following signals (*any two*):
(i) ALE (ii) HOLD (iii) IO / $\overline{M}$

(b) What is the difference between INR H and INX H instructions?

(1 + 3) + 2 + (2 × 2) + 2 = 12

3. (a) Describe the process of demultiplexing of multiplexed address-data bus (AD0-AD7) in 8085 µP with suitable circuit diagram.

(b) Write a program to find the largest number in a string of 10 byte data. Store the result in memory location 9000_H.

(c) Write the name of addressing mode used in following 8085 µP instruction —
(i) LXI H, $F000_H$ (ii) MOV A, M

4 + 6 + 2 = 12

Group – C

4. (a) With the help of timing diagram explain the sequence of events that occur for the execution of ORA M instruction. Assume that the opcode of the instruction is ZZ_H and it is stored in memory location $81FF_H$. Also calculate the time required to execute the instruction where the crystal oscillator is operated at a frequency of 4 MHz.

(b) Write a delay subroutine to generate a delay of 1.8 msec (approx.).

7 + 5 = 12

5. (a) What is the difference between maskable and nonmaskable interrupt? What is the vector location of TRAP interrupt?

(b) Draw and discuss SIM instruction format.

(c) Explain, if interrupt request is received through all the three lines —
RST 7.5, RST 6.5, RST 5.5, which of the request will be served first after the execution of following instructions:


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MVI A, 39H
SIM
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(d) With one suitable example explain the process of subroutine call.

(2 + 1) + 3 + 3 + 3 = 12

Group – D

6. (a) What is the limitation of memory mapped I/O technique?

(b) Draw the block diagram of interfacing circuit to connect 8 bit DIP switch's and 8 LED's with 8085 µP, such that the address assigned to them are $F0_H$ and $F1_H$, respectively. Write a program to read the status of the switches and display the status to the LEDs repeatedly.

2 + (5 + 5) = 12

7. (a) Write an assembly language program to determine the number of odd and even numbers from a string of 10 data bytes started at $C100_H$.

(b) What are the differences between memory mapped I/O and I/O mapped I/O schemes?

7 + 5 = 12

Group – E

8. (a) Write a program to blink a LED connected at PC_2 line of 8255 PPI. Assume a delay subroutine is available at memory location $F000_H$.

(b) Draw the block diagram of interfacing circuit to connect 8 DIP switches with 8085 µP using 8255 PPI. Write a program to count the number of switch pressed.

(c) Draw and discus CWR format of 8255 PPI in I/O.

3 + (2 + 4) + 3 = 12

9. (a) Write a program to generate square wave through counter-01 of 8254 with a frequency of 2 KHZ where the operating frequency of 8254 is 4 MHZ and A_7 address line of 8085 processor is connected to the $\overline{CS}$ pin of 8254 chip through an inverter.

(b) Write short notes on (*any two):*
(i) 8259 Programmable Interrupt Controller
(ii) 8251 USART
(iii) Interfacing of ADC with 8085 µP through 8255 PPI.

6 + 6 = 12