DIGITAL LOGIC
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) If $(361)_{10} = (551)_{b}$. Then the base b of the number is
(a) 2 (b) 9
(c) 8 (d) 5.

(ii) In which of the following adder circuits is the carry ripple eliminated?
(a) Parallel adder (b) Half-adder
(c) Carry-look ahead adder (d) Full-adder.

(iii) What is the minimum number of NAND gates required to make an XOR gate?
(a) 3 (b) 4
(c) 5 (d) 2.

(iv) A two input XOR gate can be used as an inverter when one of its input is kept at logic
(a) 0 (b) 1
(c) either 0 or 1 (d) none of these.

(v) If a function is shown as F(A, B, C, D) =Σ (1,2,4,5,8,9,10,11,15), then its compliments F' is given by
(a) F'=π(1,2,4,5,8,9,10,11,15) (b) F'=Σ (1,2,4,5,8,9,10,11,15)
(c) F'= π(0,3,6,7,12,13,14) (d) F' =Σ(0,3,6,7,8,9,10,11,15).

(vi) A Decoder with an enable input represents a functional
(a) Encoder (b) Multiplexer
(c) Comparator (d) Demultiplexer.

(vii) How many flip flops are required to design MOD-1024 counter?
(a) 1024 (b) 11
(c) 10 (d) 9.

(viii) A memory has 16 bit address bus. The number of memory locations is
(a) 16 (b) 32
(c) 1024 (d) 65536.

(ix) The capacity of a memory unit is defined by the number of words multiplied by the number of bits per word. How many separate address and data lines are needed for a memory 4K × 16?
(a) 10 addresses, 16 data lines (b) 11 addresses, 8 data lines
(c) 12 addresses, 16 data lines (d) 12 addresses, 12 data lines.

(x) The behavior of an _____sequential circuit depends upon the input signals at any instant of time *and* the order in which the inputs change.
(a) asynchronous (b) synchronous
(c) fast (d) irregular

Group – B

2. (a) A majority gate is a digital circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. Using a truth table find the Boolean function implemented by a 4 – input majority gate. Simplify the function.

(b) Given AB' + A'B = C show that AC' + A'C = B.

8 + 4 = 12

3. (a) Obtain the minimal product of sum expression for the function given below

$$f(A,BC,D) = \sum m(0,1,2,5,8,9,10).$$

(b) Prove the given Boolean expression $(A+B)(\overline{A}.\overline{C}+C)(\overline{\overline{B}+A.C}) = \overline{A}.B$.

(c) Convert the given function into canonical form $f = A.B + B.\overline{C}.D + \overline{A}.D$.

(d) Convert the numbers into desired base
(i) $(A6BF5)_{16}=(?)_2$
(ii) $(101.01)_2=(?)_{10}$.

3 + 3 + 3 + 3 = 12

Group – C

4. (a) Implement a 16:1 multiplexer using 4:1 multiplexers.

(b) Implement a full adder circuit using decoder and OR gates.

(c) Explain the operation of an octal to binary encoder.

5 + 4 + 3 = 12

5. (a) Design a 4 input priority encoder with inputs D0, (LSB) D1, D2, and D3, (MSB) and outputs Y0 Y1. Input D3 shall have highest priority and D0 shall have the lowest priority.

(b) Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the components.

6 + 6 = 12

Group – D

6. (a) Construct a D Latch with four NAND gates and an inverter.

   (b) Construct a *JK* flip-flop with universal gates of your choice and show that the characteristic equation for the complement output of the *JK* flip-flop is Q'(t + 1) = J'.Q' + J.Q.

4 + 8 = 12

7. (a) Design a synchronous MOD-6 up counter using J-K flip flop.

   (b) Explain the operation of serial in parallel out and parallel in serial out shift register.

6 + 6 = 12

Group – E

8. (a) A circuit accepts a three bit number and generates an output binary number equal to the square of the input number. Design the combinational circuit using a (8×4) ROM for this set up.

   (b) Using CMOS gates construct a two input NAND gate and explain its working principle with a truth table.

6 + 6 = 12

9. (a) Explain the basic working principle of a SRAM and a DRAM. What are their respective advantages and disadvantages? Where are they primarily used?

   (b) Implement a NOT gate using CMOS transistor?

(6 + 2 + 2) + 2 = 12